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THE DESIGN AND APPLICATION OF A NEW DIRECTIONAL COMPARISON LINE PROTECTION SCHEME TO SERIES COMPENSATED SYSTEMS

by

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BSc, AMIEE

Thesis submitted for the degree of Doctor of Philosophy of The University of Bath, 1986.

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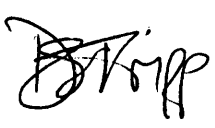

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SYNOPSIS

Series capacitors offer considerable technical and economic advantages in long distance a.c. transmission. In particular, their excellent reliability and minimal maintenance requirements make series compensation the most cost effective method of enhancing the power transfer capability of an existing or proposed interconnection.

In the late 1970s, much work was directed towards the development of new independent capacitor by-pass protection equipments to provide adequate safeguard for the capacitor banks against excessive overvoltages, particularly under fault conditions. In addition, the new generation of capacitor protection equipments, specifically those employing non-linear resistive elements, offer high-speed post-fault clearance reinsertion of the series capacitor(s), a factor of prime importance from a system stability point of view.

EHV lines employing series capacitors however, pose difficult problems for the line protection relays, not ordinarily encountered with plain feeders. One important cause of these problems is the rapid changes in circuit parameters, resulting from the operation of the capacitor protection equipment mentioned above. A further complication is introduced by the fact that the precise time at which the series capacitors are by-passed, and the number of capacitors that would be by-passed during any particular fault sequence, cannot be pre-determined. This in turn has a marked affect upon the performance of conventional line protection relays. To this end, considerable worldwide interest has been concentrated upon the development of a reliable and secure line protection scheme, specifically suited to capacitor compensated transmission systems.

The work presented herein describes the basis of a new high speed directional comparison scheme as applied to series compensated lines. The relaying principles are based upon the concept of measuring from superimposed components and are totally different from those of conventional equipment. The relay performance is examined for a variety of system and fault conditions, including systems employing non-linear capacitor bank protection. It is shown that the new relay performs satisfactorily for both internal and external faults and that it is devoid of the limitations caused by capacitor by-passing and subsequent reinsertion. For the latter purposes, realistic fault transient waveforms for a typical 500 kV series compensated system, generated using advanced time and frequency domain digital modelling techniques, are used to exhaustively test the relay.

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LIST OF PRINCIPAL SYMBOLS

A, B, C, D	Two port transmission matrices
A/D	Analogue to digital
ADC	Analogue to digital convertor
B	Circuit breaker
β	Fault angle
B1, B2	Capacitor protection circuit breakers
c	Propagation velocity
C	Capacitance
cvt	Capacitor voltage transformer
ct	Current transformer
CIM	Current input module
D	Digital division constant
DGS	Dual gap scheme
DGNS	Dual gap/non-linear resistor scheme
D(n)	Variable threshold function
DM, DR	Magnitude and rate difference functions
δ	Generator load angle
ΔT	Sampling time step
e	Time variation of voltage
$\overline{E}$	Frequency transform of voltage
$\overline{E}_{FE}$	Thevenin equivalent fault point voltage transform
ehv	Extra high voltage
fia	Fault inception angle

F,F1,F2,F3,F4,F5	Fault locations
f_{TW}	Travelling wave frequency
G	Susceptance
G1, G2	Spark gaps
γ	Propagation constant
h(t)	Unit step function
h(t-T)	Delayed unit step function
i	Time variation of current
I	Frequency transform of current
I_F	Fault current
I_L	Load current
k	Non-linear resistor characteristic coefficient
K	Source coverage gain
k_c	Gain of ADC
k_f	Gain of digital filter
k_i	Current interface gain
k_m	Modal mixing gain factor
k_o	Offset correction factor
k_v	Voltageinterface gain
k_{v2}	Voltage channel gain
k_{VP}	Voltage reflection coefficient at end P
k_{VQ}	Voltage reflection coefficient at end Q
k_{VF}	Voltage reflection coefficient at fault point
l	Line length
L	Inductance
m	Linearised curve gradient
[P]	Transmission Line matrix
p	Non-linear resistor characteristic index

ψ	Phase angle
ql	Quantum level
R	Resistance
R_F	Fault path resistance
R_1, R_2, R_3, R_4	Relay locations
R_P, R_Q	Relays at ends P, Q
R_O	Surge resistance
R_{D1}, R_{D2}, R_{D3}	Capacitor protection damping resistances
S_1, S_2	Relaying signals
scl	Short circuit level
ssr	Subsynchronous resonance
s	Laplace operator
[S]	Voltage eigenvector matrix
SGS	Single gap scheme
S_C	Degree of series compensation
S_F	Degree of series compensation during fault
t	Time
T_2, T_3	Mode 2, 3 threshold functions
T_F	Fault inception instant
T_{FO}	Capacitor flashover instant
T_{FB}	Fault break off instant
T_R	Capacitor reinsertion instant
T_{OB}	Observation time
T_{PF}	Wave transit time from P to F
T_{FQ}	Wave transit time from F to Q
θ	Phase of fault point voltage relative to end P busbar voltage

T1, T2, T3(jw)	F - domain transfer function of digital stages
T1, T2, T3(Z)	Z - domain transfer function of digital stages
T(s)	Laplace transfer function
T(n)	Threshold function
U	Unit matrix
uhs	Ultra high speed
v	Time variation of voltage
V	Frequency transform of voltage
V_C	Linearised curve intercept
V_{C1}, V_{C2}, V_{C3}	Modal voltage components
v_R	Non-linear resistor voltage
w	Angular Frequency
w_O	Nominal system angular frequency
x	Arbitrary distance
X/R	Reactance to resistance ratio
X_L	Inductive reactance
X_C	Capacitive reactance
X_{L1}, X_{L2}, X_{L3}	Capacitor protection damping reactances
[Y]	Universal admittance matrix
$[Y_O]$	Surge admittance matrix
$Y_{11}, Y_{12}, Y_{21}, Y_{22}$	Two port admittance matrices
[Z]	Universal impedance matrix
$[Z_O]$	Surge impedance matrix
$Z_{CO, 1, 2}$	Phase sequence capacitor impedances
$Z_{LO, 1, 2}$	Phase sequence line impedances
$Z_{SO, 1, 2}$	Phase sequence source impedances
Z_L	Line impedance

Z_S	Source impedance (any end)
Z_C	Series capacitor impedance
Z_T	Effective line impedance
$Z_{P,Q}$	Source impedance at end P, Q
$Z_T(w)$	Thevenin system impedance, frequency dependent
$Z_T(t-T)$	Impulse response
Z_{FE}	Thevenin equivalent fault path impedance
Z_{D1}, Z_{D2}	Capacitor protection damping impedances

Subscripts

a, b, c	Phases a, b, c
C	Capacitor
F	Fault point
P, Q	End P, Q
1, 2, 3	Mode 1, 2, 3
R	Reflected component
T	Transmitted component

Key to results figures;

a, b, c	=	three phase variables
a-e	=	'a' phase to earth fault
b-e	=	'b' phase to earth fault
b-c	=	'b' to 'c' phase fault
b-c-e	=	'b' to 'c' phase to earth fault
3ph-e	=	3 phase to earth fault
+dl	=	forward decision level
-dl	=	reverse decision level
i_2, i_3	=	mode 2, 3 current
M2, M3	=	mode 2, mode 3
ql	=	quantum level
t	=	time in milliseconds
V_2, V_3	=	mode 2, 3 voltage
x_F	=	distance to fault

CHAPTER 1: INTRODUCTION

1.1 Background and Literature Survey

The inclusion of series capacitors in a.c. transmission systems, particularly where long line sections are involved, is an effective and economic means of enhancing the power transfer capability and stability of a system as a whole. Over the years, a series capacitor employed in hv networks, has evolved into a reliable element in the transmission, achieving excellent performance and reliability standards over a number of years [1,2].

By electrically reducing the effective transmission line lengths brought about by the cancellation of part of the inductive reactance, series compensation offers the following major technical advantages over uncompensated system:-

1) The steady state power transfer capability of the network becomes proportional to the degree of series compensation. That is to say that for the maximum level of series compensation encountered in practice, typically 70%, the gain in power transfer capability is around 33%. An alternative way of looking at this is that the same level of power transfer can be achieved for a reduced load angle between the generation voltages at the line ends, thereby offering some improvement in terms of systems stability [3].

2) The voltage profile along the line is more evenly distributed under normal load conditions. This leads to a reduction in the reactive volt drops along the line, which for radially configured systems, dramatically improves the voltage regulation and hence the magnitude of the line voltages at the receiving or load ends.

3) The capacitors are self-regulative since their output voltamperes are directly proportional to the line currents flowing through them, thus improving the reactive power balance of the system.

4) Greater flexibility is introduced into the system. Power losses depend upon the line cross sectional areas and current distribution, and adjustment in the levels of series compensation help to improve the X/R ratio of the line such that transmission losses are then minimised. It should be noted that cost of introducing series capacitors or adding to existing compensation is substantially cheaper than adding new lines.

5) A switched capacitor scheme dramatically improves the transient stability limit of a system, particularly with large interconnections in which sudden losses of high loading is possible [4].

In short, the advent of series capacitor compensation has been somewhat of an economic revelation, in terms of improving the steady state transmission characteristics of a power network and reducing its transmission losses.

The cost of any power capacitor is roughly proportional to the square of the voltage that it must withstand and series capacitors become prohibitively expensive if they are to be subjected to the large voltage levels that exist during system disturbances. To protect the capacitor banks in the presence of severe overvoltages which may be developed across the capacitors, predominantly under fault conditions, three main types of independent schemes find common application worldover. These are referred to as the single-gap (SGS), dual-gap (DGS) and the dual gap/non-linear resistor (DGNS)

schemes, the fundamental purpose of each being to remove or partially remove the capacitor from the system, by by-passing or diverting the line current flowing through the latter. Each scheme employs some form of spark gap arrangement which breaks down and hence begins to conduct current, once the capacitor voltage attains a preset level, typically 2 to 3 times the nominal or steady state value.

In recent years, great technological advances have been made in the development and refinement of the capacitor protection equipments [5, 6, 7], which are described in detail in a later section. It seems likely that DGNS will become commonplace in future applications since recent publications highlight their stability boosting effect, both from a by-passing and reinsertion standpoint [5,6]. The accurate digital simulation of series compensated systems employing such schemes then constitutes a major contribution to the research of practical series compensated systems as a whole.

The action of by-passing a series capacitor results in rapid changes in the effective system impedances. Moreover, it is impossible to predict both the exact number and the precise instant in time at which the various capacitor gaps would flashover. The reason for this is that under fault conditions there are a vast number of variables which affect the magnitude of overvoltages. These include fault loop resistance, pre-fault loading, source phase sequence ratios, source capacities, type of fault, etc, as illustrated in Reference 8. Because of this degree of uncertainty, series compensated lines pose difficult protection problems for line relays. Any mode of independent tripping, without the concurrent use of signalling channels linking the protection at the two ends, is often

unsatisfactory. For example, distance relays can, depending on their settings, either overreach or underreach as a direct consequence of the operation of the series capacitor protection equipments [9].

One very common method of protecting series compensated lines involves the use of distance relays operating in a directional comparison mode in conjuction with either carrier or microwave signalling channels. In this respect, for systems with less than 50% series compensation and a capacitor located at the midpoint of the line, such a protection scheme can offer secure and reliable operation [10]. However, for economic reasons, or when the degree of series compensation is greater than 50%, the total capacitance is often split into two sections, one at each end of the line, near to, or as part of the local substations. Such locations are preferred in the USA for values of series compensation less than 50%, since the capacitors are in the vicinity of a constantly supervised area and any urgent maintenance can be carried out instantly. For such systems, directional comparison schemes using distance relays are not very satisfactory. For example, a low level fault failing to cause capacitor by-passing, can result in a loss of directionality arising as a result of voltage reversal at the relay location. In the case of double circuit applications, both voltage and current reversals are quite common. A distance relay employing a dynamic or expanding characteristic of the fully cross polarised MHO type (fcpm), goes some way to solving the inversion problem, but the degree of expansion is very dependent upon the type of fault and the impedence ratio of the local source to the series capacitive reactance [10].

Alternative proposals in relaying principles have been examined for series compensated systems, the most common types being the phase comparison and directional voltage blocking schemes. The former which are commercially available in two types, namely the segregated (phase by phase) and the phase sequence comparators, require an impedance relay to initiate the measuring process for three phase faults. However, decisions are usually based upon current components alone and the occurrence of a current inversion (leading fault current) during an internal fault, can result in phase comparator mal-operation. Furthermore, the phase sequence comparators are greatly affected by the impedance unbalance caused by unsymmetrical capacitor by-passing resulting in angular differences between the quantities at the two ends of the protected line [11]. Directional voltage blocking relays have been successfully implemented in conjunction with distance relays to block any mal-operation of the latter in the presence of voltage inversion alone. However, when both current and voltage inversion occurs, although a correct decision is available from the distance relay, nevertheless an unnecessary block is initiated by the directional voltage blocking relay. Therefore, the range of applications for which such schemes are suitable is somewhat limited.

Another approach has been adopted by Matthews and Wilkinson [12], namely a directional comparison protection suitable for compensated and plain feeder systems. A positive and negative sequence relay is provided for the detection of all types of fault, each having a trip and block element. It is designed such that for an internal fault, the trip relay operates before the block relay and overrides any action taken by the latter. The opposite procedure occurs for

external faults. There is a polarising quantity correction factor which is introduced to nullify the effect of polarising voltage inversion at the relaying point, but this factor is dimensioned upon specific ratios of the source reactance to the series capacitive reactance. This type of protection scheme would, however, find limited application in practical series compensated systems, since an effective value of source capacity and hence impedance behind the relaying points, depends entirely upon the number of infeeding lines and the number of generators connected to the local bus. Furthermore, in switched capacitor applications the ratio of the source to capacitive reactance is obviously subject to the degree of series compensation actually employed at the instant of fault.

A commonly encountered problem with series compensated line protection, arises due to the presence of sub-synchronous currents that are introduced into the system when the capacitor protective gaps do not flashover [11]. Such waveform distortions can cause improper relay operation if not catered for in the relay design. Furthermore, the resonance between the electrical system and the turbine generator mechanical system, can produce damped or undamped oscillations at the mechanical natural frequencies. Disasterous effects are possible with weak, steam turbine shafts since the high torsional stresses associated with subsynchronous resonance are of sufficient magnitude as to cause permanent shaft damage. It is

therefore of utmost importance that any line protection equipment should detect the presence of a fault on the system, with the minimum of delay. If this is achieved, rapid breaker opening could then prevent any damage to power system plant by disconnecting the faulted line section. Moreover, high speed relay operation is a desirable feature from a system stability point of view in that greater pre-fault power transfer is possible for a given system if the fault clearing time is reduced [13].

The desirable features of any line protection scheme for series compensated systems may then be summarised as follows;

a) High speed operation
b) Application independent
c) Unaffected by the action of capacitor by-passing
d) Immune to the effects of subsynchronous resonance

The foregoing considerations account, to a large extent, for ongoing interest in the development of alternative and improved methods of protection for series compensated systems. In this respect, recent years have seen the emergence of high speed directional comparison schemes in which the directional decision is initiated by relays of the travelling wave type.

Chamia and Liberman have, in conjunction with the Swedish company ASEA [14], produced a directional wave detection device called RALDA which has been installed for plain feeder field test evaluation in many countries worldover. A directional decision is based upon the relative polarities in the measured voltage and current changes at the two ends of a protected line section, the protection at the two ends being linked via a communication channel. This dependent mode of operation, configured as a blocking mode unit protection scheme is complemented with underreaching elements at each end, providing high speed independent operation, a desirable aid to rapid clearance of high level close up faults. However, such a scheme has its drawbacks in that its underlying principles are based upon an unqualified assumption. The voltage and current components are examined on a per phase basis ie segregated phase, which is perfectly acceptable for single phase networks. However, it is well known that in polyphase systems, the healthy phases, because of mutual coupling, are greatly affected by the current and voltage changes in the faulted phase. This means that under certain external fault conditions, the components induced in the healthy phases at the relaying point can be indicative of a forward or internal fault to such a scheme. When applied to series compensated systems, although such a scheme would have the distinct advantage (over conventional protection) that in a majority of practical applications, it would operate before any capacitor protective gap flashover, however, the aforementioned mutual coupling problems can be aggravated since fault current levels are generally larger for such lines than those associated with plain feeders.

In addition, a simple comparison of the relative polarities of the voltage and current changes is not a totally reliable method of determining the direction to fault when a blocking mode protection scheme is employed. A fundamental requirement of blocking schemes is that the line relay sensitivities are set so that an external fault is always detected by the blocking relay, regardless of whether the tripping or forward looking relay detects the fault or not. This prevents any unnecessary breaker opening on the protected line but introduces problems for simple polarity or magnitude comparison schemes under small signal conditions, particularly so for fault inception angles close to the voltage zerocrossing. In such cases, the initial polarities of the voltage and current changes are correctly indicative of the direction to fault for only 2 - 3 milliseconds, followed by a similar period in which they are characteristic of a fault in the other direction. Should the forward to reverse sensitivity ratio be too low, then it is feasible for the relay to render an incorrect decision. Hence the Ralda scheme, although not an impedance measuring device which makes it attractive for series compensated systems, does not however, offer total reliability of operation for all series compensated systems.

In summary then, there is to date, no known protection equipment which is attractive both from a reliability and commercial point of view that is capable of the secure protection of any arbitrary series compensated system.

It was against the above described background that work commenced on the application of the high speed directional comparison scheme, originally developed for application to plain feeders, described in Reference 15. The primary purpose of this thesis is thus to outline the progress made in the further design, development and application of the latter to series compensated lines. Particular emphasis has been paid to evolving a design that not only overcomes the foregoing practical problems but which also addresses a number of other potential problems in the application of high speed directional comparison schemes to series compensated systems.

The proposed relay, based on wave detection principles, examines the relative behaviour of two relaying signals, derived from superimposed voltage and current components at the relay locations. In this respect, it should be mentioned that the use of superimposed components instead of the total relaying point voltages and currents is logical since the steady state components are informative of the system conditions during normal operation, whereas the transient or superimposed quantities are characteristic of the fault condition alone. Furthermore, the use of superimposed quantities greatly improves the effective signal to noise ratio of the measured voltage component in the presence of capacitor voltage transformer (cvt) errors. Thus, a degree of immunity to transducer error is introduced into schemes fundamentally based upon superimposed component measurands.

The decision process however, is not performed on a segregated phase basis because of the aforementioned mutual coupling effects. Instead, the theory of natural modes as applied to polyphase systems, is employed [16]. Using mixing circuitry, the variations in the the phases are combined into modal components, which permits the complex behaviour of the system to be analysed in terms of three independent 'single phase' type circuits. For every fault condition, it is then possible to obtain a separate, unique relationship between the superimposed voltage and current for each mode at any relaying location, and hence to develop a suitable criteria for determining the direction to fault.

In order to increase the security of the new scheme in the presence of any system noise, there is a requirement that both the measured voltage and current must exceed a minimum threshold level before the decision process is initiated. Furthermore, the magnitude comparison is augmented with a check on the rate of rise of the two relaying signals, a feature which not only speeds relay operation for certain fault inception angles, but prevents any mal-operation due to differences in the forward and reverse sensitivities of the relays.

In the scheme developed, particular attention has also been paid to designing the new equipments so that the reset time of the relays is reduced to an acceptable level, thereby maximising the ability of the relays to respond to faults which are closely preceded by faults external to the protected line. This is of particular importance in applications where subsynchronous resonance components induced by faults external to the protected line may delay the resetting of the

protection. Another potential problem concerns the situation where a high level fault external to the protected line causes capacitor protection gaps to flashover which, in turn, cause a disturbance which appears internal to the protected line. Similar problems can arise following capacitor reinsertion. The special filtering and signal processing techniques that have been developed to satisfactorily deal with above mentioned problems are described.

The new high speed relay scheme is based on CAD studies and is readily implemented using present generation digital hardware. The simple and straightforward relay setting procedures developed to optimise relay performance for any practical system, make the new scheme attractive from a commercial point of view.

In the wake of a series of discussions with GEC Measurements Ltd as to the questions commonly posed by prospective consumers of power system protection equipment, the new relay has been thoroughly tested under various system fault conditions. Included in the latter are internal and external faults both close to and remote from the relaying points, for a whole range of fault inception angles. The more serious condition of an external fault causing series capacitor by-passing on the internal line section, with their subsequent reinsertion, is examined. Moreover, the performance of the relay is evaluated for each type of fault involving one or more phases. This was done despite the fact that the majority of faults on ehv systems are of the single line to ground type, in order to gain a full assessment of the relay's behaviour during both common and unusual

fault conditions. The simulation techniques used for attaining the fault transient waveforms for exhaustively testing the new relay, are essentially an extension of those described in reference 8. The thesis also describes in some detail, the complex techniques developed for accurately modelling series compensated systems incorporating various types of capacitor protection equipment, in particular those employing non-linear resistors. All of the results presented for assessing the relay performance are with respect to practical 500 kV single and double circuit systems.

1.2 Summary of the Thesis

The modelling of the series compensated networks using frequency domain analysis is outlined in Chapter 2. The techniques for representing distributed line sections by two port matrix relationships for single and double circuit systems are explained. Particular attention is paid to the simulation of external fault and their subsequent clearance from the system.

Chapter 3 concentrates again upon simulation techniques, but specifically dealing with the modelling of systems incorporating various types of independent protection equipment associated with the series capacitor banks. Great attention is focussed upon the modelling of the non-linear resistors which form an integral part of the most modern capacitor protection units. In this respect, the subtle combination of time and frequency domain analyses is explained.

The fundamental principles of the new directional relay are described in Chapter 4, which includes the derivation of relaying signals, suitable for the detection of both internal and external faults. The effects of reactive terminations at busbars directly behind the relaying locations, are analysed.

A complete breakdown of the individual stages within the new relay, as implemented in software, is given in Chapter 5. The various analogue and digital functions including pre-filtering, modal mixing, analogue to digital conversion, superimposed component extraction, digital filtering and decision processing are all explained.

In Chapter 6, the setting procedure for determining the various constants or gains for any application, is outlined. A specific example is also given for convenience. Much consideration is given to the expected levels of background noise present in relaying measurands, and how this affects the sensitivity and hence coverage of the relay.

A full relay performance evaluation is included in Chapter 7 of both single and double circuit systems. The fundamental operating principles of the new relay are explained with results of several internal and external faults involving one or more phases. Characteristics are derived for the operating times of the relay as functions of: distance to fault, fault inception angle, fault type, fault path resistance, source capacity etc. In addition, the various types of capacitor bank protections are included in order to establish any effects that they have on the relay performance, particularly when the series capacitors are reinserted into an energised system. Specific problems encountered with conventional relays applied to series compensated lines, and how the new relay overcomes them, are dealt with.

A complete summary of the advantages of the new relaying principles is given in Chapter 8 together with some proposals for future work.

CHAPTER 2: POWER SYSTEM SIMULATION TECHNIQUES

2.1 General Considerations

For the series compensated interconnection between two systems P and Q, represented by the single line diagram of Fig 2.1, mathematical and digital computation techniques have enabled the accurate simulation of fault transient phenomena and the operation of the series capacitor bank protection equipments. The source terminations are comprised of either single local generator models or a combination of the latter with some remote generation and infeeding lines. The techniques for deriving equivalent composite sources and discrete line transpositions, the latter often encountered on long lines, are fully described in Reference 20. Considering then an equivalent model of system, as shown in Fig 2.2, the simulation of a fault condition is achieved by the closure of the appropriate fault path switches in the faulted phase(s). Subsequently, the fault is removed from the system by the re-opening of those switches. The operation of the various capacitor protective gaps is simulated in a similar fashion, ie the switch in series with some damping or discharge element is closed to by-pass the capacitor bank. It must be stressed that the line section impedances of the simplified system model are in practice represented by two port ABCD networks, in order that the true distributed nature of the line is modelled.

2.2 Capacitor Bank Simulation

The model of the three phase capacitor banks, including the protective gap arrangements is illustrated in Fig 2.3. For circuit analysis purposes, it is necessary to represent such an arrangement

by an equivalent ABCD matrix and if X_L is the total pps reactance of the series compensated line section, then the capacitive reactance is related to the degree of compensation by:

$$S_C = X_C / X_L \qquad \text{--- 2.1}$$

The capacitance values per phase are then determined from a knowledge of the power frequency w_O, such that:

$$C = 1/(w_O \cdot S_C \cdot X_L) \qquad \text{--- 2.2}$$

The three phase quantities of voltage and current at either side of the capacitor bank may then be related by:

$$\begin{bmatrix} \overline{V}_1 \\ \overline{I}_1 \end{bmatrix} = \begin{bmatrix} U & Z_C \\ 0 & U \end{bmatrix} \begin{bmatrix} \overline{V}_2 \\ \overline{I}_2 \end{bmatrix} \qquad \text{--- 2.3}$$

Where each vector represents a three phase quantity, and Z_C is a 3 x 3 matrix defining the impedance of the bank, which with reference to Fig 2.3 is;

$$Z_C = \begin{bmatrix} (-jX_C + Z_{D1}) & 0 & 0 \\ 0 & (-jX_C + Z_{D1}) & 0 \\ 0 & 0 & (-jX_C + Z_{D1}) \end{bmatrix} \qquad \text{--- 2.4}$$

It should be noted that prior to the breakdown of the spark gaps (often referred to as capacitor flashover), no current flows in the impedance Z_{D2} and hence the gap potential is exactly equal to that across the capacitor/damping impedance series combination.

2.3 Frequency Domain Techniques

The transient phenomena associated with any disturbance, such as

fault or spark gap operation, represent a wide frequency variation, and it is therefore necessary to be able to evaluate the transient responses over the whole frequency spectrum. The full de-energised circuit of the system of Fig 2.2 is given in Fig 2.4, in which, each vector represents a three phase quantity and the suffix k represents the component associated with each event in the overall fault sequence. In this case the switches are replaced by current generators although in the simulation, the closure of a switch is simulated by a voltage injection, whilst switch opening is achieved by current interruption, ie by current injection.

For a three phase system, the two port ABCD matrices are determined from the distributed line parameters by application of the theory of natural modes [16]. This enables the voltages and currents at either end of a particular line section to be related as follows;

$$\begin{bmatrix} \bar{V}_1 \\ \bar{I}_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} \bar{V}_2 \\ \bar{I}_2 \end{bmatrix} \qquad \text{--- 2.5}$$

where $A = [S]\,[\cosh(\gamma l)]\,[S]^{-1}$

$B = [S]\,[\sinh(\gamma l)]\,[S]^{-1}\,[Z_O]$

$C = [Y_O]\,[S]\,[\sinh(\gamma l)]\,[S]^{-1}$

$D = [Y_O]\,[S]\,[\cosh(\gamma l)]\,[S]^{-1}\,[Z_O]$

(l = length of line section)

In order to compute the individual effects of each discrete circuit change, it is necessary to formulate a universal relationship between the forcing quantities utilising the ABCD parameters of the line, source and capacitor banks, which for the system considered takes the form:

$$\begin{bmatrix} \bar{E}_{FK} \\ \bar{E}_{CPK} \\ \bar{E}_{CQK} \end{bmatrix} = \begin{bmatrix} Z_1 & Z_2 & Z_3 \\ Z_4 & Z_5 & Z_6 \\ Z_7 & Z_8 & Z_9 \end{bmatrix} \begin{bmatrix} \bar{I}_{FK} \\ \bar{I}_{CPK} \\ \bar{I}_{CQK} \end{bmatrix} \quad \text{--- 2.6}$$

In Eq 2.6, each sub marix Z_1, Z_2, ..., Z_9 is of the order 3 x 3, the elements of which are evaluated from the two port equivalent circuit relationships. Appendix A2.1 contains the analysis for determining the sub-matrices above and Eq 2.6 may be expressed in full three phase form as follows;

$$\begin{bmatrix} \bar{E}_{Fka} \\ \bar{E}_{Fkb} \\ \bar{E}_{Fkc} \\ \bar{E}_{CPka} \\ \bar{E}_{CPkb} \\ \bar{E}_{CPkc} \\ \bar{E}_{CQka} \\ \bar{E}_{CQkb} \\ \bar{E}_{CQkc} \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} & Z_{15} & Z_{16} & Z_{17} & Z_{18} & Z_{19} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} & Z_{25} & Z_{26} & Z_{27} & Z_{28} & Z_{29} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} & Z_{35} & Z_{36} & Z_{37} & Z_{38} & Z_{39} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} & Z_{45} & Z_{46} & Z_{47} & Z_{48} & Z_{49} \\ Z_{51} & Z_{52} & Z_{53} & Z_{54} & Z_{55} & Z_{56} & Z_{57} & Z_{58} & Z_{59} \\ Z_{61} & Z_{62} & Z_{63} & Z_{64} & Z_{65} & Z_{66} & Z_{67} & Z_{68} & Z_{69} \\ Z_{71} & Z_{72} & Z_{73} & Z_{74} & Z_{75} & Z_{76} & Z_{77} & Z_{78} & Z_{79} \\ Z_{81} & Z_{82} & Z_{83} & Z_{84} & Z_{85} & Z_{86} & Z_{87} & Z_{88} & Z_{89} \\ Z_{91} & Z_{92} & Z_{93} & Z_{94} & Z_{95} & Z_{96} & Z_{97} & Z_{98} & Z_{99} \end{bmatrix} \begin{bmatrix} \bar{I}_{Fka} \\ \bar{I}_{Fkb} \\ \bar{I}_{Fkc} \\ \bar{I}_{CPka} \\ \bar{I}_{CPkb} \\ \bar{I}_{CPkc} \\ \bar{I}_{CQka} \\ \bar{I}_{CQkb} \\ \bar{I}_{CQkc} \end{bmatrix}$$

--- 2.7

Simulation of the transient phenomena is then achieved by imposing constraints upon the relevant voltage and current vectors for a particular kth event, and computing the components generated by that disturbance alone. Since for the system considered there are many such disturbances which may occur during the fault sequence, the universal matrix elements are calculated and stored at each frequency. In this way the computational demands are reduced since although for a given system, the universal matrix elements are frequency variant, the overall relationship between the forcing quantities at any particular frequency, is fixed and as such the same matrix may be re-used with the appropriate constraints for each subsequent kth event.

The foregoing analysis may be extended to include circuit breaker

simulation at busbars P and Q as described by Kalam [19], by increasing the order of the matrix [Z], such that;

$$\begin{bmatrix} \overline{E}_{Fk} \\ \overline{E}_{CPk} \\ \overline{E}_{CQk} \\ \overline{E}_{BPk} \\ \overline{E}_{BQk} \end{bmatrix} = [Z] \begin{bmatrix} \overline{I}_{Fk} \\ \overline{I}_{CPk} \\ \overline{I}_{CQk} \\ \overline{I}_{BPk} \\ \overline{I}_{BQk} \end{bmatrix} \qquad \text{--- 2.8}$$

Where $\overline{E}_{BPk}$, $\overline{E}_{BQk}$, $\overline{I}_{BPk}$, $\overline{I}_{BQk}$ are the kth terms of the end P and Q breaker voltage and current components respectively. In this instance, the order of [Z] is 15 x 15. Moreover, a double circuit configuration, without circuit breaker simulation, is again modelled in a similar way, with the size of the universal matrix now increased to 18 x 18 and to 30 x 30 if circuit breaker action is required.

2.4 Simulation of Changes in Circuit State

The fundamental principle employed in the simulation of the discrete changes in circuit state is that of superposition, achieved with the aid of the aforementioned frequency domain techniques. At the commencement of the overall fault sequence simulation it is essential to establish the steady state variations at the relevant points within the system, for which k=1. Subsequently, k=2 corresponds to the first change in circuit state, for example fault inception, possibly followed by the operation of one of the capacitor spark gaps whereby k is increased to 3. The total variation of voltage or current at any point is then determined by simply summating the time domain variations as k increases from 1 to n, where n is the number of discrete circuit changes. The steps involved in establishing each

kth component are best explained with reference to a typical fault sequence, and the following analysis is relevant to the specific case of an 'a' phase to ground fault, followed by the operation of the 'a' phase capacitor protection at end P (Fig 2.4).

2.4.1 Steady State Analysis

During the prefault condition (k=1), the voltages and currents at all points within the system are fixed by the busbar voltages $\overline{V}_P$ and $\overline{V}_Q$. With no currents flowing in the fault path nor in the spark gap branches, the circuit of Fig 2.4 is reduced to that of Fig 2.5, in which the line parameters are calculated at the system power frequency. Since the busbar voltages are set according to power transfer requirements, the source impedances do not affect the steady state currents $\overline{I}_{P1}$ and $\overline{I}_{Q1}$ and as such, the busbar arrangements are represented by voltage generators. From the diagram, the following relation is available;

$$\begin{bmatrix} \overline{V}_{P1} \\ \overline{I}_{P1} \end{bmatrix} = \begin{bmatrix} A_{PC} & B_{PC} \\ C_{PC} & D_{PC} \end{bmatrix} \begin{bmatrix} A_C & B_C \\ C_C & D_C \end{bmatrix} \begin{bmatrix} A_{CC} & B_{CC} \\ C_{CC} & D_{CC} \end{bmatrix} \begin{bmatrix} A_C & B_C \\ C_C & D_C \end{bmatrix} \begin{bmatrix} A_{CQ} & B_{CQ} \\ C_{CQ} & D_{CQ} \end{bmatrix} \begin{bmatrix} \overline{V}_{Q1} \\ \overline{I}_{Q1} \end{bmatrix} \quad \text{--- 2.9}$$

or $$\begin{bmatrix} \overline{V}_{P1} \\ \overline{I}_{P1} \end{bmatrix} = \begin{bmatrix} A_E & B_E \\ C_E & D_E \end{bmatrix} \begin{bmatrix} \overline{V}_{Q1} \\ \overline{I}_{Q1} \end{bmatrix} \quad \text{--- 2.10}$$

Hence with $\overline{V}_{P1}$ and $\overline{V}_{Q1}$ being known specified busbar voltages, $\overline{I}_{Q1}$ and $\overline{I}_{P1}$ are readily found;

$$\overline{I}_{Q1} = B_E^{-1}(\overline{V}_{P1} - A_E.\overline{V}_{Q1})$$
$$\text{and } \overline{I}_{P1} = C_E.\overline{V}_{Q1} + D_E.\overline{I}_{Q1} \quad \text{--- 2.11}$$

The prefault fault point voltage vector, $\overline{V}_{F1}$, which is necessary for the fault transient simulation, is determined from the sub-relationship given below, assuming that the fault is at Point F indicated in Fig 2.5;

$$\begin{bmatrix} \overline{V}_{F1} \\ \overline{I}_{F1} \end{bmatrix} = \begin{bmatrix} A_{CC} & B_{CC} \\ C_{CC} & D_{CC} \end{bmatrix} \begin{bmatrix} A_C & B_C \\ C_C & D_C \end{bmatrix} \begin{bmatrix} A_{CQ} & B_{CQ} \\ C_{CQ} & D_{CQ} \end{bmatrix} \begin{bmatrix} \overline{V}_{Q1} \\ \overline{I}_{Q1} \end{bmatrix} \quad \text{--- 2.12}$$

or $$\begin{bmatrix} \overline{V}_{F1} \\ \overline{I}_{F1} \end{bmatrix} = \begin{bmatrix} A_E & B_E \\ C_E & D_E \end{bmatrix} \begin{bmatrix} \overline{V}_{Q1} \\ \overline{I}_{Q1} \end{bmatrix} \quad \text{--- 2.13}$$

Thus $\overline{V}_{F1}$ is calculated from the known vectors $\overline{V}_{Q1}$ and $\overline{I}_{Q1}$ determined in Eq 2.11, such that;

$$\underline{\overline{V}_{F1} = A_E . \overline{V}_{Q1} + B_E . \overline{I}_{Q1}} \quad \text{--- 2.14}$$

Since no current flows in the fault path prior to fault inception, then $\overline{E}_{F1}$ is equal to $\overline{V}_{F1}$.

Similar two port relations are available for the calculation of the prefault voltages across the series capacitors, $\overline{E}_{DP1}$ and $\overline{E}_{DQ1}$, with the latter terms being equal to those across the spark gaps $\overline{E}_{CP1}$ and $\overline{E}_{CQ1}$, since $\overline{I}_{CP1}$ and $\overline{I}_{CQ1}$ are zero.

2.4.2 Fault Transient Analysis

The simulation of the phase to ground fault condition is achieved by injecting a voltage component designated $\overline{E}_{F2a}$, at the fault point,

from the instant of fault inception, T_F. The time domain expression for this forcing quantity is given by;

$$e_{F2a} = -\overline{E}_{F1a} \sin(w_O t + \beta)h(t-T_F) \qquad \text{--- 2.15}$$

which describes a voltage equal and opposite to the prefault variation, finite after time T_F with the fault inception angle β given by $(w_O \cdot T_F)$ and zero for all time up to T_F. Since the above quantity is a sinusoid, a Laplace transform of Eq 2.15 enables the frequency spectrum of the forcing voltage to be found as follows;

$$\overline{E}_{F2a} = -\overline{E}_{F1a} \cdot [w_O \cdot \cos\beta + jw \cdot \sin\beta]/(w_O^2 - w^2) \qquad \text{--- 2.16}$$

At the instant of fault inception on the 'a' phase, the healthy phase fault path currents are zero as are all six currents in the spark gap branches, thus;

$$\overline{I}_{F2b,c} = \overline{I}_{CP2a,b,c} = \overline{I}_{CQ2a,b,c} = 0$$

These known zero valued transforms, when substituted in the universal matrix of Eq 2.7 then yield the following relation;

$$\overline{E}_{F2a} = Z_{11}\, \overline{I}_{F2a}$$

$$\text{or} \quad \overline{I}_{F2a} = Z_{11}^{-1} \cdot \overline{E}_{F2a} \qquad \text{--- 2.17}$$

Hence the fault path current in the faulted phase is determined from the forcing quantity $\overline{E}_{F2a}$, and when re-substituted into Eq 2.7, all other state k=2 voltages are found. Thus the voltages at all points of interest which are generated by the fault point forcing voltage acting alone are calculated in this way.

The frequency domain profiles of the variables are then mapped into the time domain via Modified Fourier methods as described in Reference 17. With regard to the end P 'a' phase series capacitor, the total, open circuit gap potential, equal to that of the series capacitor/damping impedance combination is given by;

$$e_{CPa}(t) = e_{CP1a}(t) + e_{CP2a}(t-T_F) \qquad \text{--- 2.18}$$

where $e_{CP2a}(t)$ is the prefault capacitor voltage and $e_{CP2a}(t-T_F)$ is the fault induced component.

2.4.3 Capacitor Spark Gap Operation

The computer simulation of the fault condition yields the total time domain voltage variations across the series capacitors and hence their open circuit spark gaps. By comparing the gap potentials with a pre-defined threshold level, it it then possible to determine if any of the spark gaps would operate and in which order. Thus, unsymmetrical gap flashover on the faulted phase(s) is modelled, taking each operation in turn, increasing k at each stage. If the 'a' phase capacitor gap potential at end P is the first to exceed the threshold, then the time and corresponding frequency variations of the required forcing voltage, with k=3, are given by;

$$e_{CP3a} = -(e_{CP1a} + e_{CP2a})h(t-T_{CP})$$

$$\text{and } \overline{E}_{CP3a} = \int_{T_{CP}}^{T_{OB}} e_{CP3a} \cdot \exp(-jwt)dt \qquad \text{--- 2.19}$$

At this point it is worth mentioning that the change in spark gap state from open to short circuit is modelled by a simple switch

closure. In practice however, arcing between the gap electrodes is possible, a phenomena which in itself is highly non-linear, but of secondary importance to the actual closure of the gap branch. Hence, the open/close switch simulation detracts very little from the physical condition in terms of accuracy.

By consideration of the circuit state with k=3, it is possible to isolate the zero valued transforms with the circuit again de-energised. In this case the latter terms are;

$$\overline{E}_{F3a} = \overline{I}_{F3b,c} = \overline{I}_{CP3b,c} = \overline{I}_{CQ3a,b,c} = 0$$

The previous spark gap currents associated with the end P 'a' phase capacitor are zero ($\overline{I}_{CP1a} = \overline{I}_{CP2a} = 0$), but after flashover, $\overline{I}_{CP3a}$ and the new component in the fault path $\overline{I}_{F3a}$, generated by the applied forcing voltage, are determined from the sub-relationship of Eq 2.20, in this instance making use of the universal admittance matrix described in Appendix A2.1;

$$\begin{bmatrix} \overline{I}_{F3a} \\ \overline{I}_{CP3a} \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} 0 \\ \overline{E}_{CP3a} \end{bmatrix} \qquad \text{--- 2.20}$$

where $\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{14} \\ Z_{41} & Z_{44} \end{bmatrix}^{-1}$

Therefore;

$$\overline{I}_{F3a} = Y_{12} \cdot \overline{E}_{CP3a}$$

and $\overline{I}_{CP3a} = Y_{22} \cdot \overline{E}_{CP3a}$ --- 2.21

Again by re-substitution of these currents into the universal relation of Eq 2.7, the flashover induced components at all other

points may be determined. Then by invoking the inverse frequency transform, the time domain variations for state k=3 are obtained, which are added to previous components to yield the total variations. The most likely proceeding disturbance for the case considered, is the flashover of the 'a' phase capacitor at the other end of the line section, ie at Q. The analytical expression for the total time varying voltage across the gap potential up to the point at which the latter exceeds the threshold, is given by;

$$e_{CQa}(t) = e_{CQ1a}(t) + e_{CQ2a}(t-T_F) + e_{CQ3a}(t-T_{CP})$$

The foregoing superposition technique is repeated until no further gap operations occur.

The damping impedances considered above Z_{D1} and Z_{D2}, are passive linear elements and as such can be modelled in the frequency domain. However, in the current state of the art capacitor protection schemes, the damping circuit comprises chiefly of a non-linear resistor in series with the spark gap. The simulation of spark gap breakdown in such situations is no longer achieved by application of a forcing quantity to a frequency dependent system matrix, but by involving a subtle combination of time and frequency domain techniques. The subject in itself is worthy of a detailed analysis and is described in detail in the next chapter.

2.5 External Fault Simulation

Hitherto, the analysis has been concentrated upon the sequence of events following a fault internal to the line section P-Q. For

example, a fault on busbar P is represented by the equivalent model of Fig 2.6. If however, a fault occurs at some point say within system P, this constitutes an external fault condition with respect to the series compensated line section. This in turn may cause the internal capacitor protection to operate, expecially if modern, low setting dual gap protection schemes are employed, thereby posing a threat to the system stability. Such a sequence of events is of concern to the power system line protection engineer since it occurs whilst the series compensated line is energised during the entire external fault cycle. It is therefore of the utmost importance to simulate such conditions so that any proposed line protection equipments may be subjected to waveforms containing the superimposed components generated by each event.

A single line diagram illustrating an external fault condition with fault location F, on an infeeding line R-P, with some local source at P and remote source at R, is shown in Fig 2.7. The equivalent two port network of Fig 2.8 is constructed for this situation, in which the location of a circuit breaker B, just behind busbar P is indicated. By application of Thevenin's theorem to this circuit, equivalent fault point quantities $\overline{E}_{FE}$ and Z_{FE}, observed at B, may be derived from the original terms $\overline{E}_F$ and R_F. With the breaker open, the open circuit voltages $\overline{E}_{FE}$ are calculated from the application of $\overline{E}_F$ at the fault point and then by de-energising the infeeding line section (set $\overline{E}_F$ to zero), an equivalent impedance Z_{FE} looking towards end R may be found. The process involved in determining the Thevenin equivalent terms are described in Appendix A2.2, from which;

$$Z_{FE} = (A_{FP} \cdot Z_E + B_{FP})\ (C_{FP} \cdot Z_E + D_{FP})^{-1} \qquad \text{--- 2.22}$$

and $$\overline{E}_{FE} = A_{FP}^{-1}[U + R_F \cdot Z_{FF}^{-1}] \cdot \overline{E}_F \qquad \text{--- 2.23}$$

where $$Z_E = [(C_{RF} \cdot Z_R + D_{RF})\ (A_{RF} \cdot Z_R + B_{RF})^{-1} + Y_F]^{-1}$$

and $$Z_{FF} = -([(C_{FP} \cdot A_{FP}^{-1}) + (C_{RF} \cdot Z_R + D_{RF})(A_{RF} \cdot Z_R + B_{RF})]^{-1} + R_F)$$

Thus the equivalent terms are derived solely as functions of the line and source parameters of the section R-P. The equivalent circuit, showing in detail the arrangement at busbar P, including the Thevenin terms $\overline{E}_{FE}$ and Z_{FE} is then shown in Fig 2.9, whereby it is apparent that the circuit now resembles exactly that of Fig 2.6. Thus the transient analysis for the internal fault case may then be executed as before by the straightforward substitution of $\overline{E}_{FE}$ for $\overline{E}_F$ and Z_{FE} for R_F. In addition, the equivalent fault currents $\overline{I}_{FE}$ now resemble those line currents which would flow through circuit breaker B, feeding the section R-P. Hence the superposition techniques may then be applied to interrupt either one or all three phase currents flowing through breaker B, thereby disconnecting the fault from the system with respect to the series compensated line section. Following the clearance of such a fault, the line current levels within the section P-Q would greatly diminish, thus permittng the reinsertion of the capacitor(s) which have been previously by-passed.

2.6 Double Circuit System Simulation

The foregoing analysis applies to a single circuit configuration, but could be extended for double circuit applications, with an associated doubling of the order of the universal matrices. For series elements such as the compensating capacitors, the circuit

analysis necessary for the formulation of the universal matrix is relatively straightforward, when two port ABCD networks are employed. However, certain disadvantages arise with such methods when multi-parallel paths such as infeeding lines and outfeeds are involved, particularly so for double circuit systems. An alternative, straightforward approach for such systems is to make use of two port Y parameter relationships to derive the universal matrix, in which admittances representing parallel paths are simply added. Moreover, the Y parameter elements are more accurate for higher sampling frequencies which are required for very detailed analysis of the initial post fault period. There is of course a drawback with respect to series elements being represented by Y parameters and for this reason, a double circuit system has been simulated with the mathematical formulation based upon a combination of the ABCD and Y parameters of the system elements.

The majority of line protection problems associated with double circuit series compensated systems arise as a result of the capacitors staying in circuit for the duration of the fault. Hence, invaluable information is gained, concerning the performance of line protection equipments as applied to double circuit configurations, by simulating fault conditions on either circuit, but excluding the operation of the capacitor bank protection equipments.

2.6.1 Uncompensated Double Circuit Formulation

A plain feeder double circuit interconnection linking two ends P and Q, with several infeeds at either end, is shown in Fig 2.10. Such an arrangement has, for faults on either circuit, a universal relation of the form;

$$\begin{bmatrix} \overline{I}_{F1} \\ \overline{I}_{F2} \\ \overline{I}_{P} \\ \overline{I}_{Q} \end{bmatrix} = [Y] \begin{bmatrix} \overline{V}_{F1} \\ \overline{V}_{F2} \\ \overline{V}_{P} \\ \overline{V}_{Q} \end{bmatrix} \qquad \text{--- 2.24}$$

The universal system admittance matrix [Y] is of the order 12 x 12 and is derived from a two port Y parameter equivalent of the system which is shown in Fig 2.11. The terminating admittances Y_P and Y_Q behind the busbars are in fact the sum of all local and infeeding admittance terms. The individual two port networks Y_{PF} and Y_{FQ} are derived from the basic homogeneous line section relationships, which with reference to Fig 2.12 are of the form;

$$\begin{bmatrix} \overline{I}_1 \\ \overline{I}_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} \overline{V}_1 \\ \overline{V}_2 \end{bmatrix} \qquad \text{--- 2.25}$$

where $Y_{11} = Y_O\,[S][\coth(\gamma l)][S]^{-1}$

$Y_{12} = -Y_O\,[S][\operatorname{cosech}(\gamma l)][S]^{-1}$

$Y_{21} = Y_{12}$

and $Y_{22} = Y_{11}$ (for homogeneous line section)

Barker [21] describes in detail, the procedure for determining the elements of the universal matrix from the above parameters. Such a technique is then developed to incorporate series capacitors into the line section, as described below.

2.6.2 Midpoint Series Compensation

With series capacitors located in the middle of the double circuit line section, providing all of the series compensation, the ABCD matrix is of the form;

$$\begin{bmatrix} A_C & B_C \\ C_C & D_C \end{bmatrix} = \begin{bmatrix} U & X_C \\ 0 & U \end{bmatrix} \qquad \text{--- 2.26}$$

The equivalent two port network of the system, assuming that the fault location is closer to P than Q, is then drawn in Fig 2.13. The ABCD parameters of the line sections and the series capacitor bank are then combined, which reduces the equivalent network to the form of Fig 2.11 ie;

$$\begin{bmatrix} A_{FQ} & B_{FQ} \\ C_{FQ} & D_{FQ} \end{bmatrix} = \begin{bmatrix} A_{FC} & B_{FC} \\ C_{FC} & D_{FC} \end{bmatrix} \begin{bmatrix} A_C & B_C \\ C_C & D_C \end{bmatrix} \begin{bmatrix} A_{CQ} & B_{CQ} \\ C_{CQ} & D_{CQ} \end{bmatrix} \qquad \text{--- 2.27}$$

This ABCD representation may be transformed into a Y parameter equivalent via the procedure for parameter conversion outlined in Appendix A2.3. Hence the system as a whole is then treated as if it were uncompensated, with the analysis for a plain feeder system then being applicable.

2.6.3 Compensation Near Line Ends

For double circuit systems employing series compensation which is split into two, with a capacitor bank location at each end of the interconnection, ther ABCD parameters for each bank are as follows;

$$\begin{bmatrix} A_C & B_C \\ C_C & D_C \end{bmatrix} = \begin{bmatrix} U & X_C/2 \\ 0 & U \end{bmatrix} \qquad \text{--- 2.28}$$

Once again a similar equivalent network to that of Fig 2.11 may be obtained by simple multiplication of the capacitor banks, giving equivalent ABCD networks on either side of the fault point. Hence, from Fig 2.14, for the left hand side;

$$\begin{bmatrix} A_{PF} & B_{PF} \\ C_{PF} & D_{PF} \end{bmatrix} = \begin{bmatrix} U & X_C/2 \\ 0 & U \end{bmatrix} \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \quad \text{--- 2.29}$$

and

$$\begin{bmatrix} A_{FQ} & B_{FQ} \\ C_{FQ} & D_{FQ} \end{bmatrix} = \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} U & X_C/2 \\ 0 & U \end{bmatrix} \quad \text{--- 2.30}$$

for the right hand side.

The equivalent Y parameters formed from the ABCD matrices PF and FQ then enable the derivation of the aforementioned universal matrix, with fault simulation carried out as for the plain feeder case.

The above techniques allow the calculation of the system faulted behaviour, which is the prime objective of the work, without the provision of the capacitor protection operation. However, it is suggested that some useful research may be carried out into the complete simulation of such systems incorporating all of the facilities already employed in the single circuit case, despite the highly complex combination of series and parallel formulations and high order matrices that are involved.

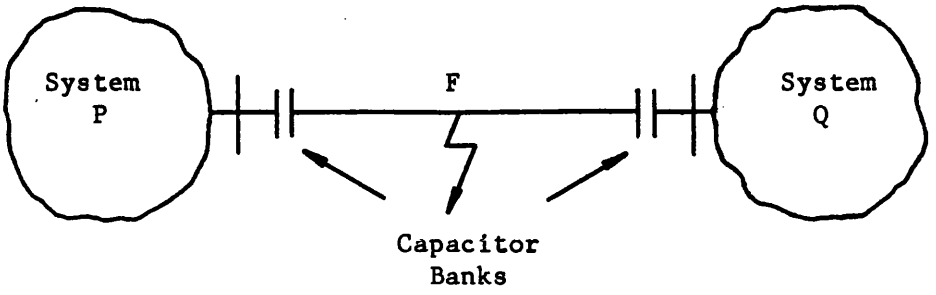


Fig 2.1 Series Compensated System

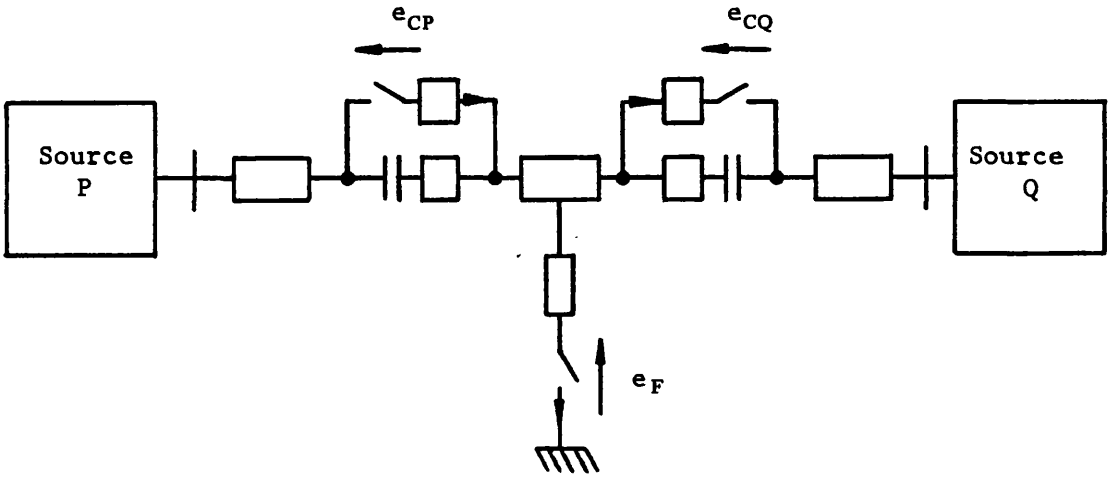


Fig 2.2 De-energised model for fault and capacitor by-pass simulation

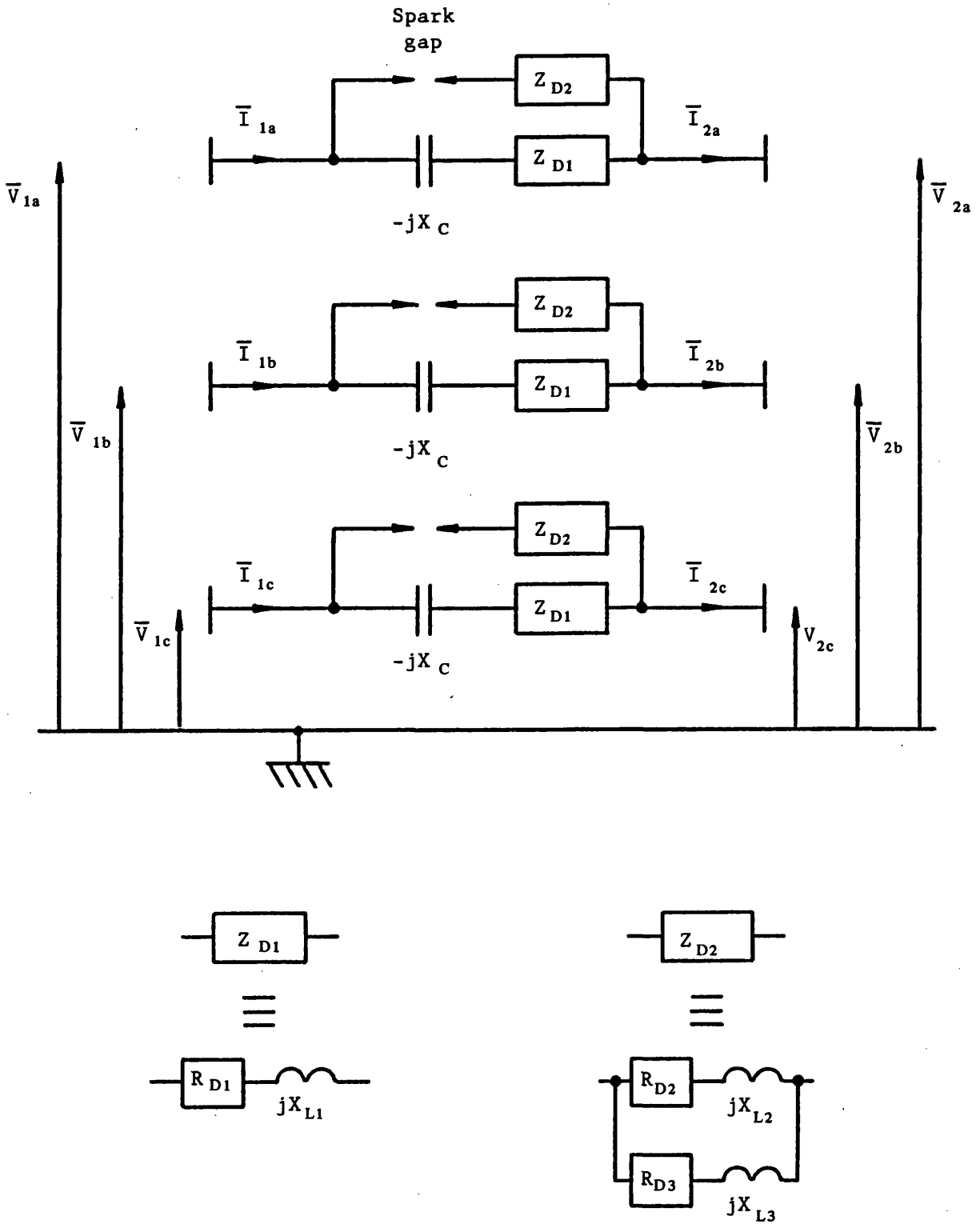


Fig 2.3 Series Capacitor Bank Protection Arrangements

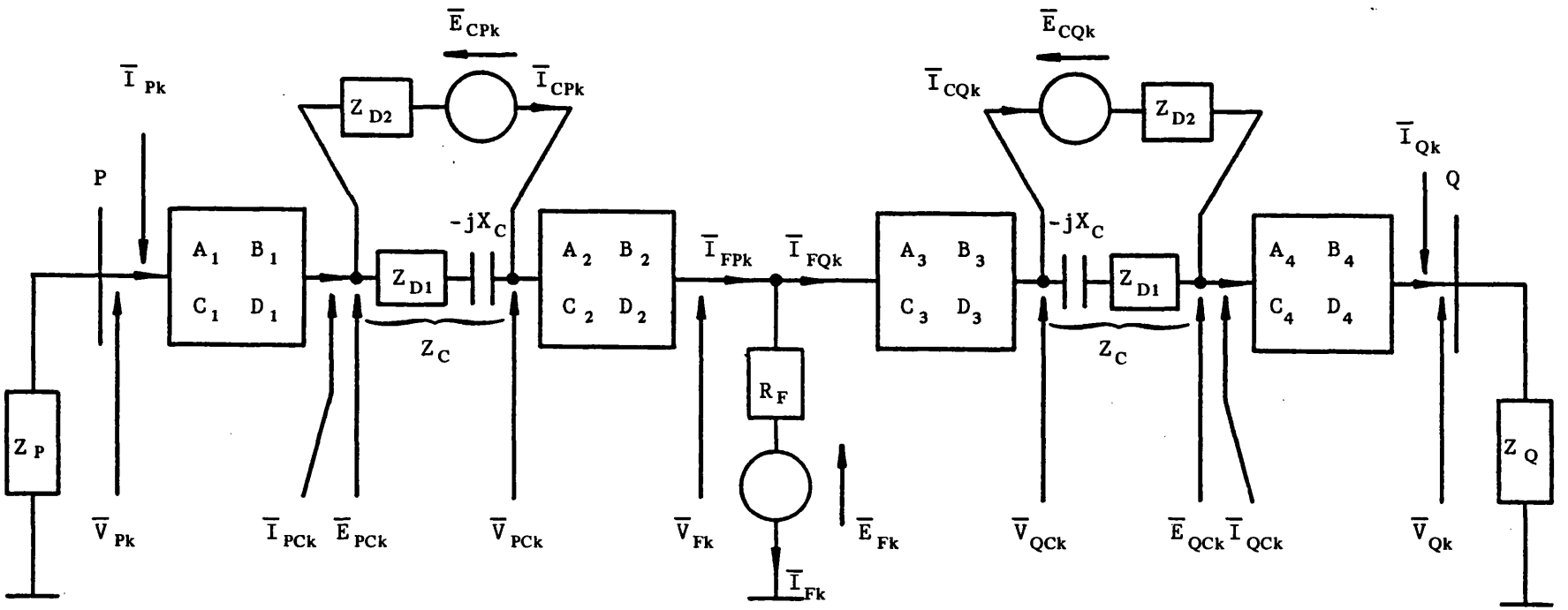


Fig 2.4 Frequency domain superimposed-system model

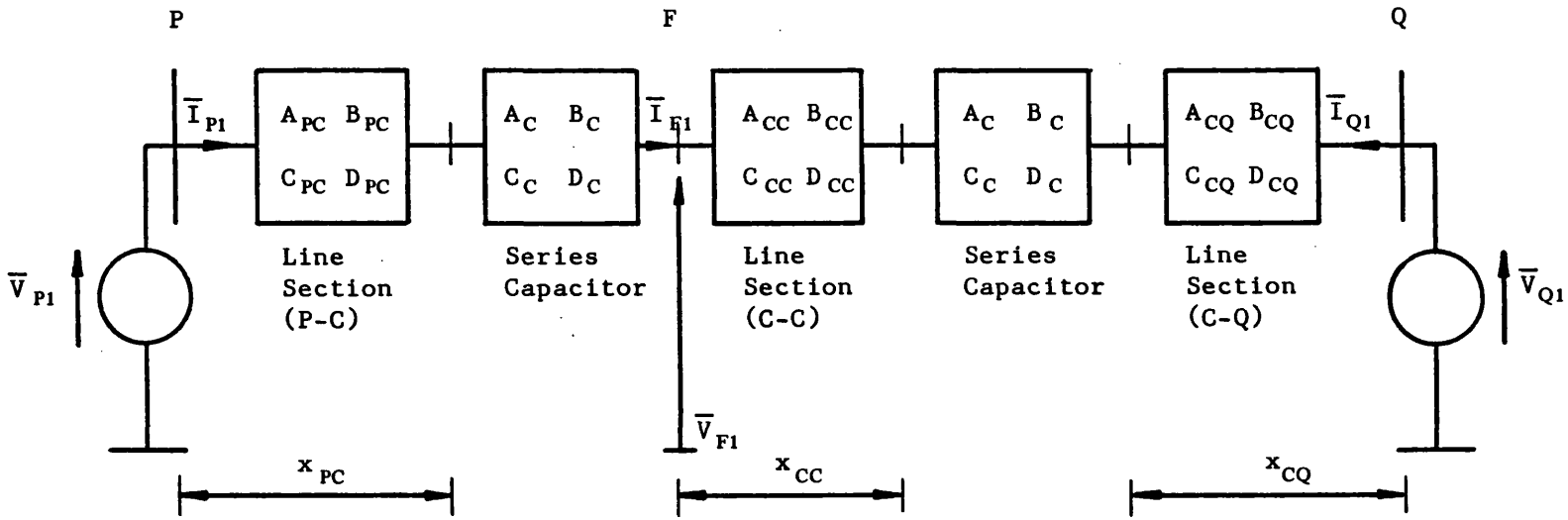


Fig 2.5 Steady State (k=1) prefault model

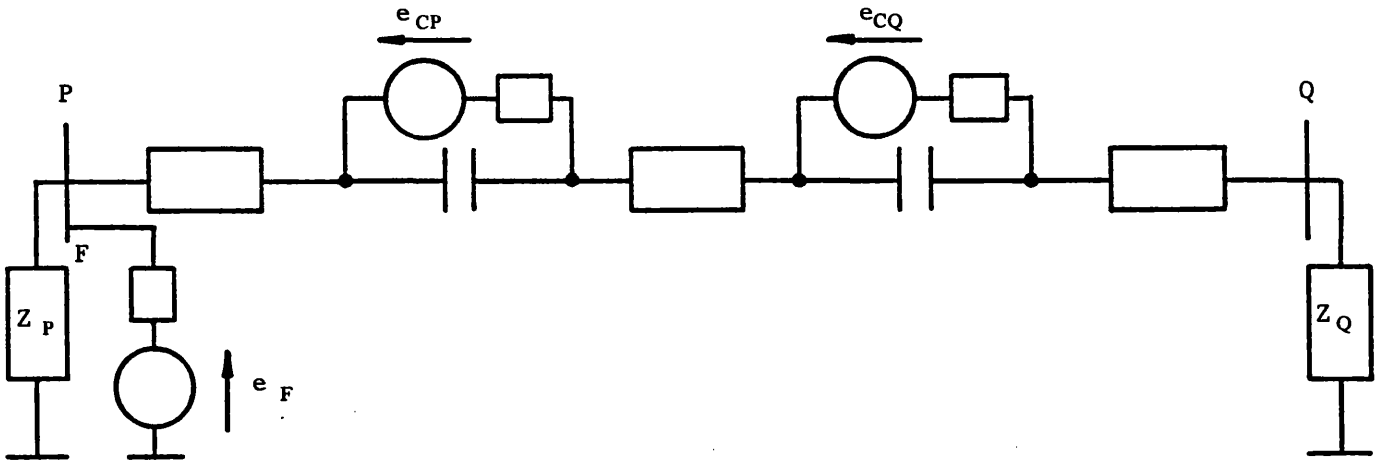


Fig 2.6 De-energised system model - fault on busbar P

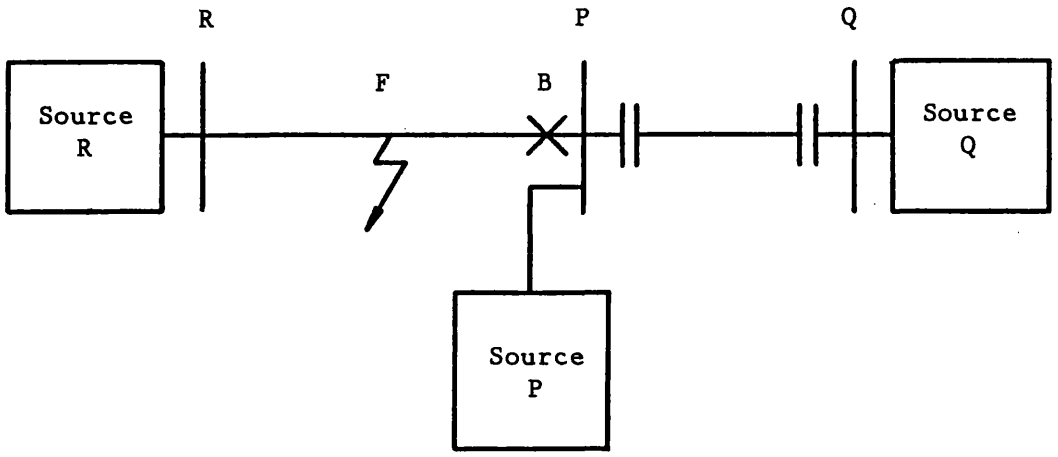


Fig 2.7 System model for external fault

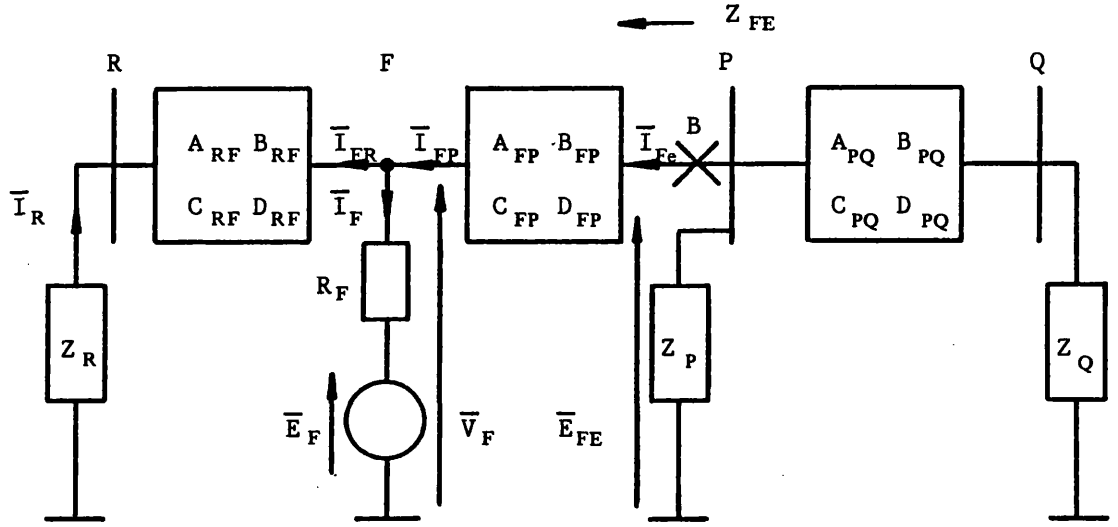


Fig 2.8 De-energised system model for external fault

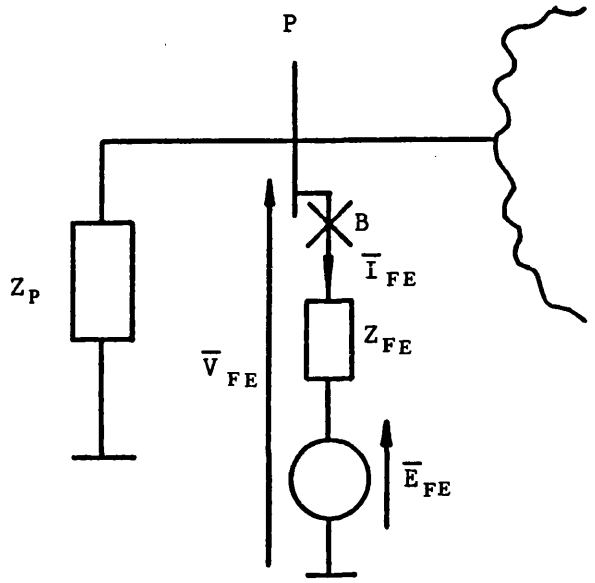


Fig 2.9 Thevenin equivalent circuit of Fig 2.8, Showing end P arrangement in detail

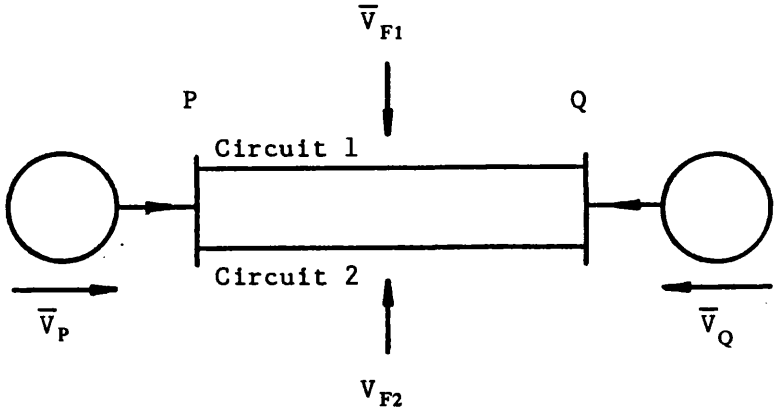


Fig 2.10 Uncompensated double circuit system

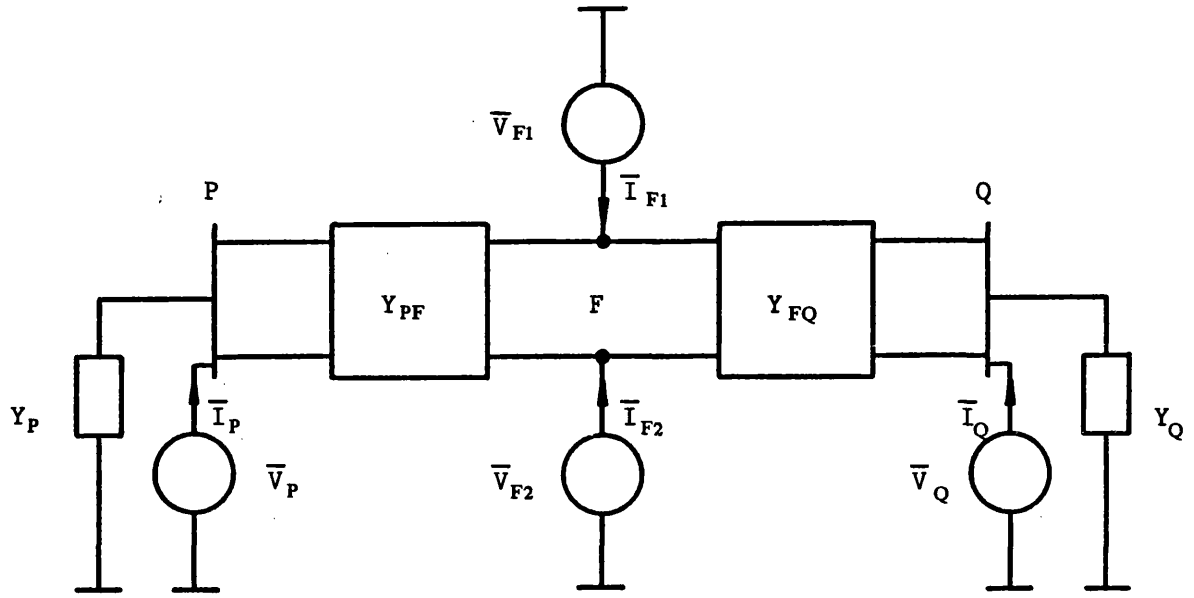


Fig 2.11 Two port 'Y' parameter representation of uncompensated double circuit system

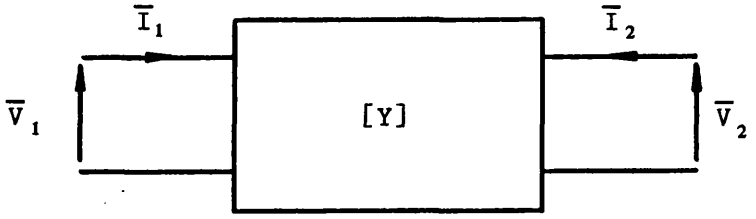


Fig 2.12 General 'Y' parameter two port equivalent circuit

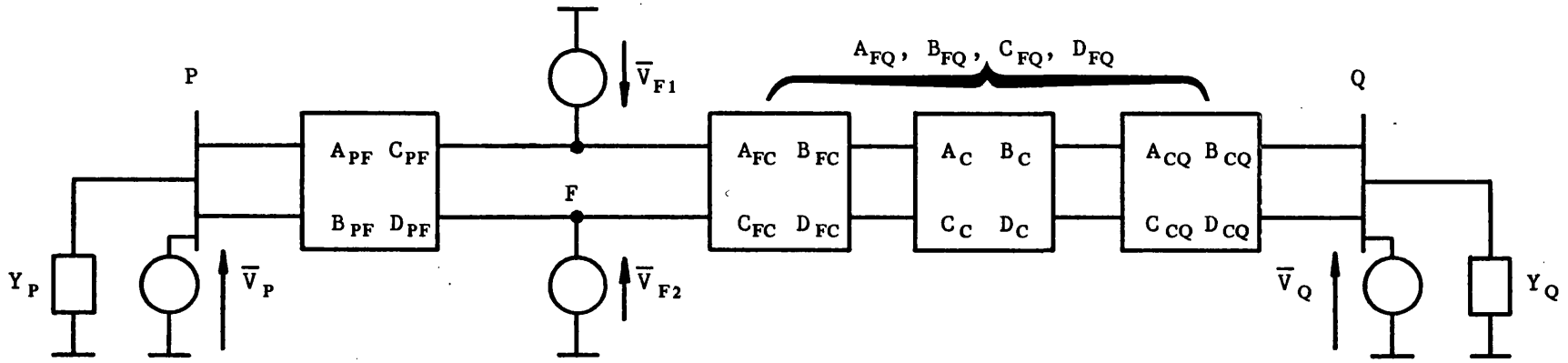


Fig 2.13 Two port equivalent of series compensated double circuit system (Compensation at midpoint, fault near P)

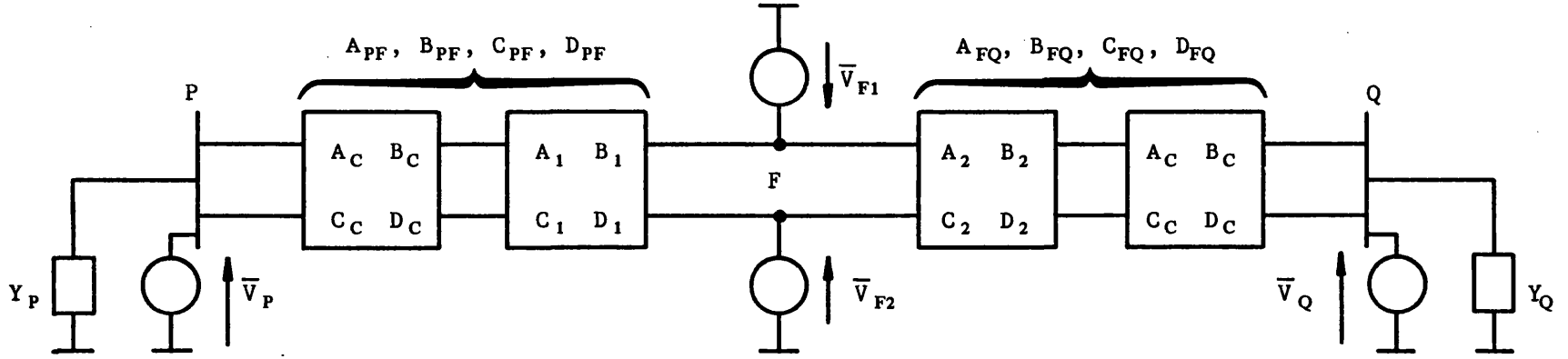


Fig 2.14 Two port equivalent of series compensated double circuit system with compensation at line ends

CHAPTER 3: SERIES CAPACITOR PROTECTION SCHEMES

3.1 Introduction

During the period of a disturbance on a power system, particularly under fault conditions, severe overvoltages may be developed across each item of plant. The most common countermeasure employed to prevent permanent damage is the use of surge arrestors or divertors. For reasons of greater speed of operation and high speed reinsertion however, series capacitors are individually protected by means of some form of spark gap arrangement [22]. Three types of capacitor protection schemes find common worldwide application which are broadly classified as follows;

1) The single gap scheme (SGS).
2) The dual gap scheme (DGS).
3) The dual gap/non-linear resistor scheme (DGNS).

The fundamental objective of the capacitor protection is to by-pass or shunt the capacitor with a low impedance path, thus preventing excessive voltages being developed across them. Once the capacitor voltage attains a certain threshold level, the spark gap breaks down or in other words is triggered into conduction, thereby connecting a branch usually comprising of a discharge limiting resistor and inductor, in parallel with the capacitor. Most of the line current is then diverted through this parallel path and away from the series capacitor. Such an arrangement then forms the most basic type of capacitor protection, commonly referred to as a single gap scheme (SGS), as shown in Fig 3.1, and as described in Chapter 2.

Ideally, the spark gap threshold level should be set high enough such that all faults external to the series compensated line section do not cause by-passing of the capacitors. However, the major limitation of this is that the cost of a series capacitor is roughly proportional to the square of the voltage that it must withstand. With today's large integrated power networks and associated high fault current levels at most points within them, the cost of the capacitors then becomes prohibitively expensive if the gap settings are to prevent by-passing for all external faults. The reason for concern that the internal capacitors may be by-passed for external faults lies in the fact that for the same power demand from the series compensated line section, the increased transfer reactance due to capacitor by-passing poses a threat to the system transient stability as a whole.

Subsequent developments in the design of capacitor bank protection has led to the adoption of the dual gap scheme (DGS), this being a direct development from the SGS. The basic SGS is modified by the inclusion of an additional branch comprising an extra spark gap and a series circuit breaker. The second gap (referred to as the auxilliary gap) has a lower setting than the original gap (referred to as the main gap), thereby allowing capacitor by-pass under external fault conditions. The advantages of such a scheme are best understood by consideration of the method by which both schemes perform reinsertion. With the SGS, the parallel breaker (Fig 3.1) is used to short out the main gap branch and hence to divert the current away from the latter. The gap then extinguishes and subsequently

deionises, regaining it's normal open circuit condition. Capacitor reinsertion is then achieved by the reopening of the parallel breaker. This method suffers two major drawbacks as detailed below;

1) The parallel breaker, usually of the oil minimum type, has a typical closing time of about 5 cycles, with a further 1.5 cycles required for contact separation. The SGS has therefore, an inherent delay at the initiation and completion of the reinsertion cycle.

2) The time required for the spark gap to sufficiently deionise is dependent upon various factors which include environmental conditions, state of the gap electrodes and fault current levels. Once the parallel breaker is opened, the voltage stress lies across the main gap, which if not fully deionised, may restrike at voltage level appreciably below the original preset value. For fault currents below 10 kA, a deionisation time of around 10 cycles after breaker closure is required to ensure adequate recovery of the gap withstand capability and this in turn hinders high speed post-fault reinsertion of the capacitors.

A further consequence of having a high gap setting is the capacitors would remain in circuit during most external fault conditions and indeed for internal faults involving highly resistive fault paths. Thus, the chance of interaction between the electrical and mechanical systems producing subsynchronous currents, which may be initiated by any power system disturbance, is therefore greatly increased.

The SGS has however, proven to be a very reliable and robust element in overseas countries, with excellent service histories being reported [5,6]. In cases where the capacitor bank installations are situated in remote geographical locations, thus causing obvious maintenance problems, and in systems in which external fault levels are relatively low, it is thought that the SGS will remain as the standard method of achieving capacitor protection. It is however, the poor, slow speed reinsertion capability of the SGS which precludes the latter from being a suitable protection in large integrated networks.

With the second or auxilliary gap having a lower setting, the DGS permits by-passing for lower fault levels. The instances of by-passing are more prevalent, but the DGS is capable of much faster reinsertion then the SGS, thus reducing the risk of system instability. Fig 3.2 shows the simplified arrangement of a DGS and in this case it is the series breaker (B2) which performs the reinsertion. Due to the lower gap setting of G2 compared with that of the main gap G1, this branch operates first to by-pass the capacitor. After fault clearance, the breaker B2 open circuits the dual branch, leaving the original main gap protecting the capacitor in the event of any subsequent overvoltage. In this instance, the main gap G1 is termed a 'clean' gap, since it has not previously conducted any by-pass current and so has a well defined voltage withstand level. The voltage stress in this case is totally placed upon the series breaker and not upon a spark gap, and high speed reinsertion is possible since a single opening action is required rather than the much slower close/open cycle with deionisation delay of the SGS.

The gap setting of a SGS is typically around 2.7 pu of the nominal or steady state capacitor voltage. With a corresponding lower gap setting of a DGS around 2.2 pu, this constitutes a capital saving in the region of 33%. Therefore, the DGS offers both an improvement in the stability of the system by means of high speed reinsertion and large economic savings in terms of capital investment.

The above schemes shunt the capacitor with a low impedance path, which although is frequency dependent, its values of inductance and resistance are constant and linear. This results in practically all of the compensating reactance being lost for the by-pass duration. As mentioned previously, the effect of this is to cause an increase in the effective transfer reactance of the series compensated line section, thereby posing stability problems. An ideal situation would then be to shunt the capacitor in such a way as to only partially remove the compensating reactance, whilst retaining full protection against overvoltages. This is achieved by inserting a non-linear resistor in series with the dual gap branch to form the dual gap/non-linear resistor scheme, DGNS, as shown in Fig 3.3, and as originally proposed in Reference 5. The impedance in the shunt path varies in sympathy with the voltage developed across the capacitor/resistor combination, producing a self-regulative action, holding the capacitor voltage to an acceptable level, whilst merely reducing the compensation as opposed to losing it altogether with the other schemes. A simple analysis of the steady state fault condition, whereby only power frequency components are considered, enables a simple expression to be developed for the effective change in the degree of series compensation. The ratio of the capacitive

reactance to the line pps impedance yields the steady state prefault degree of compensation;

$$S_C = X_C/X_L \qquad \text{--- 3.1}$$

For the SGS or the basic DGS, the whole of the compensation is lost during by-passing, hence the variation is described by;

$$S_C \rightarrow 0 \rightarrow S_C \qquad \text{--- 3.2}$$

However, the corresponding cycle of the DGNS may be described by;

$$S_C \rightarrow S_F \rightarrow S_C \qquad \text{--- 3.3}$$

S_F being a fraction of S_C ie, $S_F = S_C/(1+(X_C/R)^2)$, R being the resistance of the non-linear resistor.

The variation of R with the time varying voltage across it causes the degree of compensation to change between S_C (R very large) and some smaller quantity dependent upon the minimum value of R. During the faulted period therefore, the transfer reactance of the series compensated line section is not so dramatically increased as with the SGS or DGS, the overall effect of this being to reduce the acceleration of the supply generators.

To illustrate the above effects, power transfer curves for the system of Fig 3.4 may be constructed, as shown in Fig 3.5. During steady state conditions, normalised power transfer curves are identical for both the DGS and DGNS and are based upon the standard equation;

$$P = E_P \cdot E_Q \cdot \sin(\delta)/X_T \qquad \text{--- 3.4}$$

Where E_P and E_Q are the generator line voltages, δ is the load angle between the two ends and X_T is the transfer reactance given by $X_L - X_C$. Now assuming that 50% series compensation is employed and that a fault at F results in the by-passing of the capacitors, X_T then doubles (X_C falls to zero) for the DGS. Hence for a given input power P_{IN}, Fig 3.5a indicates that area 1 is larger than area 2, which if the equal area criterion is applied, reveals that such a situation poses a threat to the system stability. However, by appropriate selection of the non-linear characteristic, a corresponding curve for the DGNS scheme is obtained as shown in Fig 3.5b. For the case considered, an average degree of compensation of just less than 30% during the period of fault is applicable, and it is clearly evident that area 1 is now substantially less than area 2, thus removing the threat of instability.

By consideration of a series equivalent circuit of the capacitor/non-linear resistor combination, a time variant series resistance, dependent upon the non-linear characteristic may be determined. Hence a desirable series damping element is introduced into the line section which considerably reduces the magnitude and effects of any subsynchronous currents which may be present on the system. Indeed because of this damping effect, the non-linear resistor reduces all of the switching transients associated with capacitor bank protection equipment.

After fault clearance, the line currents and hence the magnitude of the voltage across the series capacitor/non-linear resistor combination falls. The compounding effect of the non-linear characteristic is that the current in the by-pass branch diminishes to an even lower level. Thus almost immediately after fault clearance, most of the line current is transferred back through the series capacitor. This then constitutes an automatic reinsertion of the capacitor, without the need for any breaker switch action at all. The series breaker is then opened some time later to extinguish the gap although the opening delay is no longer critical since very high speed reinsertion has already been achieved. In addition, the stresses placed upon the series breaker in the DGNS are minimal due to the very low current levels which it is required to interrupt.

In summary, the inclusion of a non-linear resistor as part of the dual gap branch, introduces the following capacitor protection advantages;

1. Very high speed reinsertion.
2. Improved compensation during the faulted period.
3. Increased damping of subsynchronous components.
4. Reduced stress upon capacitor protection breakers.
5. Reduced switching transients.

3.2 Simulation

In order to assess the effects of capacitor by-passing the reinsertion upon the fault transient waveforms, particularly at relaying locations, the operation of each type of capacitor

protection scheme was simulated. The frequency domain techniques described in Chapter 2 are applied to the SGS and the DGS, whereas a combination of time and frequency domain analyses is required for the DGNS model.

For each case, the total voltage developed across the capacitors in each phase, is checked against a preset threshold value. Once the threshold is exceeded, the digital techniques for simulating the operation of the spark gaps, ie, the opening and closing of the switches, are involked as described below.

3.2.1 SGS

The operation of the SGS in summary, involves the injection of a voltage across the gap terminals equal and opposite to the open circuit gap potential, a technique fully described in Chapter 2.

3.2.2 DGS

In Section 3.1 it was made clear that the lower gap setting of the DGS is beneficial to the financial aspects of the capacitor installations. However, there is an associated increase in the number of by-passing operations which the DGS must then make. From a simulation point of view however, the by-passing action of the DGS is exactly the same as for a SGS since the series breaker is in the normally closed position (Fig 3.3). Hence the only difference in the modelling of the two schemes is the lower preset threshold value of the spark gap in a DGS and in some cases slightly different values of damping parameters.

3.2.3 DGNS

The simulation of a DGNS by-pass action involves a more complex process than a simple voltage injection. It is essentially a hybrid combination of the time and frequency domain techniques, developed for secondary arc simulation work by Johns and Al-Rawi [23].

Typicalvoltage/current characteristics of a silicon carbide and a zinc oxide non-linear resistor are depicted in Fig 3.6, whereby the voltage is a function of the current which in turn is a function of time, hence.

$$v_R(t) = f(i(t),t) \qquad \text{--- 3.4}$$

and typically; $$v_R(t) = k.i(t)^p \qquad \text{--- 3.5}$$

From the universal system matrix, described in Chapter 2, the effective or Thevenin impedance, $Z_T(w)$, looking into the system from the capacitor terminals, with all voltage sources set to zero, is readily found. (See Appendix A3.1). For one particular capacitor, the frequency domain equivalent circuit is then drawn as in Fig 3.7. The latter is constructed on the assumption that no other capacitors have previously been by-passed, ie all other by-pass currents are zero. The voltage balance relationship of the circuit is then simply;

$$\overline{V}_R = \overline{E}_C - Z_T.\overline{I} \qquad \text{--- 3.6}$$

This frequency domain equation cannot be solved since the voltage and current through the resistor can only be related in time. However, Eq 3.6 is readily transformed into an equivalent time domain expression via Fourier methods;

$$v_R(t) = e_C(t) - \mathcal{F}^{-1}(Z_T.\bar{I}) \qquad \text{--- 3.7}$$

or $$v_R(t) = e_C(t) - \frac{1}{2\pi}\int_{-\infty}^{\infty}(Z_T.\bar{I})e^{jwt}\ dw \qquad \text{--- 3.8}$$

The integral part of Eq 3.8 is solved by application of the convolution theorem, such that;

$$v_R(t) = e_C(t) - \int_{-\infty}^{\infty} Z_T(t-\tau)i(\tau)\ d\tau \qquad \text{--- 3.9}$$

where $$Z_T(t-\tau) = \frac{1}{2\pi}\int_{-\infty}^{\infty} Z_T.e^{jw(t-\tau)}\ dw \qquad \text{--- 3.10}$$

and τ is a dummy variable of integration.

Equation 3.10 is representative of the impulse response of the system or in other words, the function $Z_T(t-\tau)$ describes the voltage variation that would be produced across the capacitor terminals due to the injection of a unit impulse of current into $Z_T(w)$. Since a real, causal physical system is under consideration, the function $Z_T\ (t-\tau)$ must be zero for $t-\tau < 0$ or $t < \tau$. Furthermore, the time $t = 0$ can be defined as the precise instant of by-passing such that;

$$i(t) = 0 \text{ for } t < 0 \qquad \text{--- 3.11}$$

The modified integral limits are then applied to Eq 3.9 such that;

$$v_R(t) = e_C(t) - \int_{o}^{t} Z_T(t-\tau)i(\tau)\ d\tau \qquad \text{--- 3.12}$$

or $$e_C(t) = v_R(t) + \int_{o}^{t} Z_T(t-\tau)i(\tau)\ d\tau \qquad \text{--- 3.13}$$

Any digital simulation analyses time responses on a sample by sample basis and the forcing function $e_C(t)$ and the impulse response $Z_T(t-\tau)$ are obtained in discrete samples using Fourier transform techniques, referred to in Chapter 2. Moreover, the expression of Eq 3.4 may now be introduced to enable the solution of Eq 3.13, to be made from the instant of by-passing until the end of the observation period, this being split into 'n' steps of width 'ΔT'. Thus;

$$e_C(t) = f(i(t),t) + \int_o^{n\Delta T} Z_T(t-\tau)i(\tau)\, d\tau \qquad \text{--- 3.14}$$

Now the integral part of Eq 3.14 is numerically evaluated by simple trapezoidal techniques at 't' increases from 0, ΔT, $2\Delta T$, ..., $n\Delta T$, such;

$$\int_o^{n\Delta T} Z_T(t-\tau)i(\tau)\, d\tau = (\text{first + last ordinates})/2 + (\text{sum of all others})$$

or in analytical terms;

$$\int_o^{n\Delta T} Z_T(t-\tau)i(\tau)\, d\tau = \left\{ \left[\frac{Z_T(o)i(n)+Z_T(n)i(o)}{2} \right] + \left[\begin{array}{l} Z_T(1)i(n-1)+Z_T(2)i(n-2) \\ + \ldots \ldots + Z_T(n-1)i(1) \end{array} \right] \Delta T \right\} \qquad \text{--- 3.15}$$

ie
$$\int_o^{n\Delta T} Z_T(t-\tau)i(\tau)\, d\tau = \frac{Z_T(o)i(n)\Delta T}{2} + \frac{Z_T(n)i(o)\Delta T}{2} + \sum_{k=1}^{n-1} Z_T(n-k)i(k)\Delta T \qquad \text{--- 3.16}$$

At the instant of by-pass, the circuit resembles a simple R-C charging network, with the capacitor acting as a short circuit. Thus the first current sample i(0) is therefore only limited by the non-linear resistance, ie $i(0) = e_C(0)/R$.

The summation part of Eq 3.16 is valid for $n > 2$, but for $n = 1$, it is zero hence Eq 3.14 becomes;

$$e_C(1) = f(i(1),1) + \left[\frac{Z_T(o)i(1) + Z_T(1)i(o)}{2}\right]\Delta T \qquad \text{--- 3.17}$$

and for $n > 2$;

$$e_C(n) = f(i(n),n) + \left[\frac{Z_T(o)i(n) + Z_T(n)i(o)}{2}\right]\Delta T \qquad \text{--- 3.18}$$
$$+ \sum_{k=1}^{n-1} Z_T(n-k)i(k)\Delta T$$

A knowledge of the characteristic behaviour of f(i(1),1) enables Eq 3.17 to be solved for i(1) since $e_C(1)$, $i(0)$, $Z_T(0)$, $Z_T(1)$ and ΔT are known quantities. Subsequently for $n > 2$, the summation only involves previous values of current i (k), that is for the jth calculation, only terms upto j-1 are required. Hence n = 1 initiates a recursive method, establishing a starting point for the total solution upto time = $n\Delta T$. With the foregoing considerations in mind, when solving Eq 3.18 at any particular sample, the summation is therefore effectively a constant. Moreover, the terms $Z_T(0).\Delta T/2$ and $Z_T(n).\Delta T/2$ appear in each calculation and as such may also be taken as constants. Rewriting Eq 3.18 then gives;

$$e_C(n) = f(i(n),n) + C.i(n) + D + X \qquad \text{--- 3.19}$$

where $C = Z_T(0).\Delta T/2, D = Z_T(n).i(0).\frac{\Delta T}{2}$ and $X = \sum_{k=1}^{n-1} Z_T(n-k)i(k)\Delta T$

The quantity f(i(n),n) is now considered in detail remembering that this represents the non-linear resistor voltage as a function of the current. By piecewise linearisation of the characteristic of Fig 3. 6 , simple linear equations of the form y = mx + c are obtained. The detailed Fig 3.8 shows a sub-divided characteristic with three main areas described by;

$i < i_1$ ------ A

$i_1 < i < i_2$ ------ B

$i > i_2$ ------ C

Once the current i(n) is determined from Eq 3.19, the corresponding voltage $v_R(n)$ and the associated slope and intercept values are then readily obtained. The accuracy of the linearisation obviously depends upon the number of sub-divisions which are taken and the technique is valid only if the current is actually flowing in the resistor. Hence at the precise instant of by-passing, the current flowing in the by-pass branch, is assumed to be $e_C(0)/R$, which enables the evaluation of the first sample value of f(i(1),1). Given that the open circuit condition of the branch results in no potential difference across the resistor, prior to by-passing, it is assumed that the slope of the characteristic is the greatest value ie $m = m_1$. Once the step voltage is applied to simulate the spark gap operation, the current quickly achieves its correct value and any error introduced by the original estimation is quickly swamped.

The above method then allows the resistor voltage to be expressed in the form;

$$v_R(n) = f(i(n),n) = V_C + m.i(n) \qquad \text{--- 3.20}$$

where V_C is the current intercept value and m the corresponding slope.

Now substitution of Eq 3.20 into Eq 3.19 yields;

$$e_C(n) = V_C + m.i(n) + C.i(n) + D + X \qquad \text{--- 3.21}$$

or $$i(n) = (e_C(n) - V_C - D - X)/(m + C) \qquad \text{--- 3.22}$$

Given any sample of the forcing voltage $e_C(n)$, the corresponding sample of current in the by-pass branch, i(n) is found. Again it is emphasised that when n = 1, X = 0 and from the linearised resistor characteristic, values of v_R and m are determined from the first resistor current sample i(0), hence;

$$i(1) = (e_C(1) - V_C - D)/(m + C) \qquad \text{--- 3.23}$$

In order to establish the effects of inserting the non-linear resistor across the capacitor, upon the rest of the system, the same digital process as that for the SGS is employed, with the forcing voltage $e_C(t)$ replaced by $[e_C(t) - v_R(t)]$. The frequency transform of the latter quantity is then applied to the system universal matrix as before.

The foregoing describes the simulation of one capacitor by-pass operation only. For the SGS and the DGS any subsequent by-passing is achieved simply by setting the forcing voltage in the first by-pass branch to zero. In other words, the system is again de-energised and the new forcing voltage in the second by-pass branch determines the superimposed components at all points within the system. Unfortunately, such a straightforward approach is not applicable for the DGNS simulation due again to the fact that the non-linear resistor voltage and current cannot be related as a function of frequency. The non-linear path formed by the first by-pass must be opened at the instant that the second capacitor voltage exceeds the threshold level. This is only a temporary, but necessary measure to enable the correct voltage profile across the second capacitor, over the whole observation period, to be determined.

At this stage it is worth describing the method by which the by-pass branches are opened by each scheme. This action interrupts all current in the by-pass branch thereby reinserting the capacitor into the system. The general arrangement is shown in Fig 3.9 whereby the current is injected into the capacitor terminals from an ideal source in series with some impedance quantity, D. Because an ideal source is used, it is irrelevant whether the latter consists of linear or non-linear elements, the current flowing into the capacitor terminals is exactly the same as that generated by the current source. This technique is therefore suitable for each type of capacitor protection scheme.

Returning to the DGNS scheme, the sequence of events up until the second capacitor voltage exceeds the threshold level is then;

1. First capacitor by-pass at $t = T_{CP}$, associated superimposed components added to total variations at all points.

2. Second capacitor voltage > threshold at $t = T_{CQ}$. First branch is opened at $t = T_{CQ}$, associated superimposed components added as above.

Both capacitor by-pass branches are now closed simultaneously and it must be stressed that in practice, the first branch would remain closed for the whole period, it is only for computational reasons that it is temporarily opened. Now as two forcing voltages are applied simultaneously to the circuit, this demands the simultaneous solution of time domain equations to determine the resistor voltages. For mathematical convenience, it is an advantage to redefine time $t = 0$ as the instant of second capacitor by-pass ie T_{CQ} becomes time zero. The procedure for determining the resistor voltages is described in Appendix A3.2 and the injection process then involves two quantities given by;

$$\bar{E}_{CP} = \mathcal{F}\{(e_{CP}(t) - v_{RP}(t))\}$$
$$\text{and} \qquad \bar{E}_{CQ} = \mathcal{F}\{(e_{CQ}(t) - v_{RQ}(t))\} \qquad \text{--- 3.24}$$

3.2.3.1 External Line Circuit Breaker Opening

For the special case described in Chapter 2 whereby a single line to ground fault occurs on an external line section causing the internal capacitor by-passing, single pole opening to clear the fault with respect to the compensated line, is achieved simply for the SGS or DGS. Once again however, the non-linear paths of the DGNS must be

temporarily opened and reclosed as above. With the non-linear path(s) open, a current injection applied to the circuit then simulates the pole opening as described in the previous Chapter. The effect of this is that the impedance term $Z_T(w)$, ie, the Thevenin impedance looking into the capacitor terminals, is modified due to the change in the state of the system. Using the new $Z_T(w)$ and hence impulse response, the by-pass branches are reclosed again with time zero redefined to be the instant of pole opening. Appendix A3.1 includes the calculations for finding the Thevenin impedances both with and without the faulted phase breaker pole closed.

3.3 Simulation Results

Figs 3.10 to 3.12 illustrate the desirable features of the DGNS for a line to ground fault at the point F in Fig 3.4. The faulted phase line currents of Fig 3.10, common to both ends of the system, show that for a high gap setting associated with a SGS, substantial subsynchronous modulation is dominant. With the DGS, some of the subsynchronous current is attenuated, due to the large step increase in the transfer reactance, which also causes the magnitude of the line current to fall. With the DGNS however, the subsynchronous component is all but eliminated and the line current is observed to be approximately 400 amps higher than that with the DGS. Waveforms associated with the capacitor bank closest to the fault are given in Fig 3.11, from which it is seen that the DGS causes the capacitor voltage to be clamped to almost zero. The DGNS however, adequately protects the capacitor against overvoltage, whilst maintaining a substantial voltage across the latter. A comparison of the by-pass

branch currents of Fig 3.11c and d, shows that the magnitude of the switching transient of the DGS is approximately 5 times that of the DGNS, a result further emphasised by the detailed waveforms of Fig 3.12a. After the fault is cleared, Fig 3.12b shows that for the DGS, a substantial current (500 A peak) flows in the gap branch, whereas for the DGNS, at approximately 20 milliseconds after fault clearance, the current diminishes virtually to zero. The series capacitor would, in the latter case, then be almost fully reinserted without the necessity of interrupting the gap branch current.

Of the three schemes described, the DGNS is thus the most attractive since it boosts the transient stability of a series compensated system, whilst offering economic savings by way of reducing the withstand requirements of the capacitors.

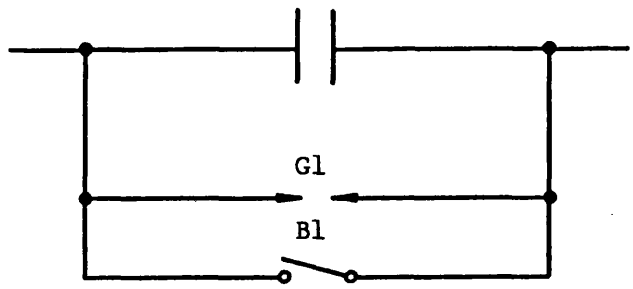


Fig 3.1 Single gap scheme (SGS)

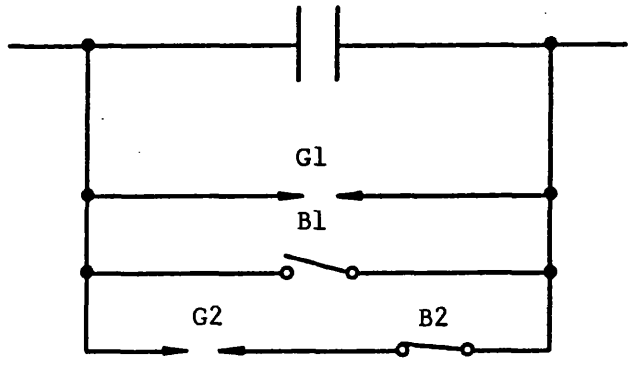


Fig 3.2 Dual gap scheme (DGS)

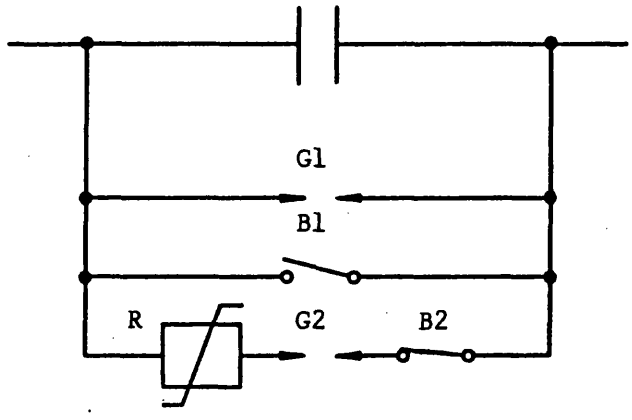


Fig 3.3 Dual gap/non-linear resistor scheme (DGNS)

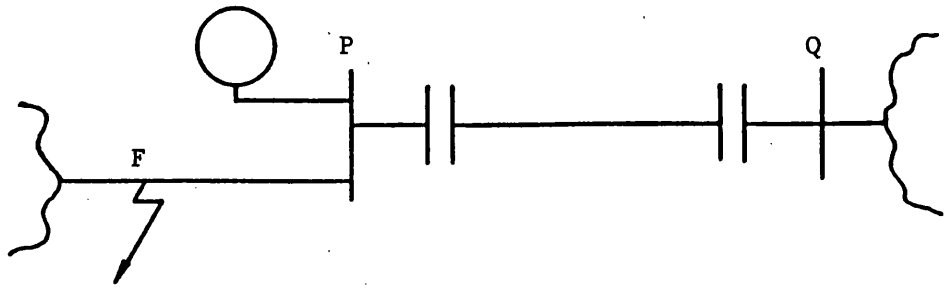
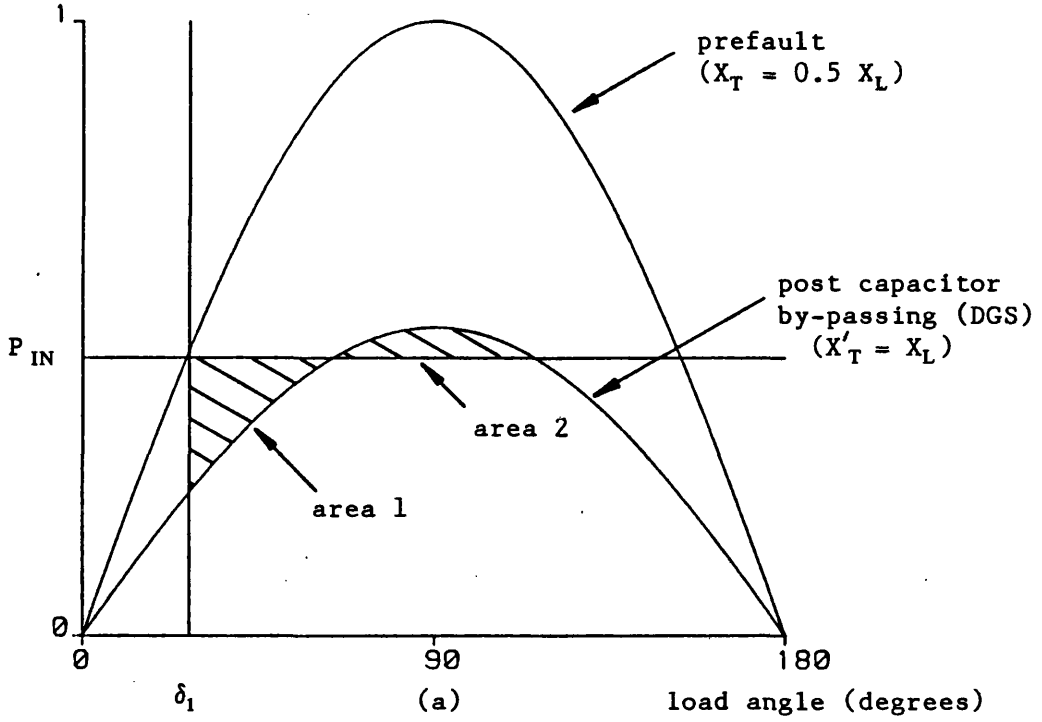


Fig 3.4 Series compensated system for DGS and DGNS comparisons



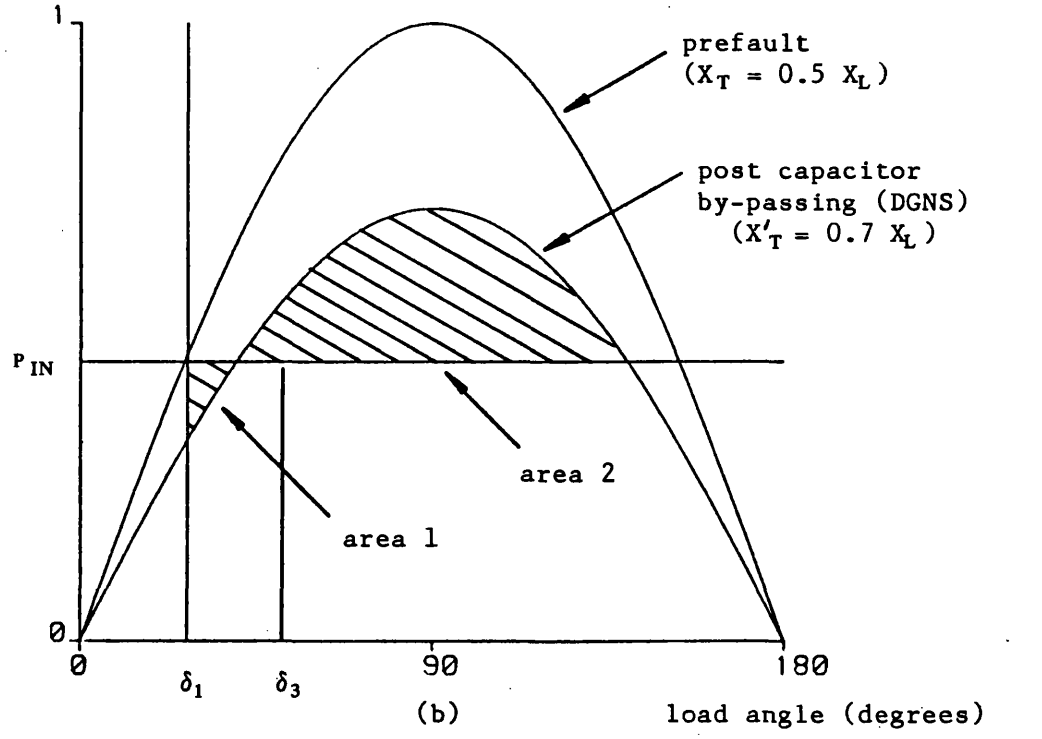


Fig 3.5 Power transfer curves for system of Fig 3.4, before and after capacitor by-passing

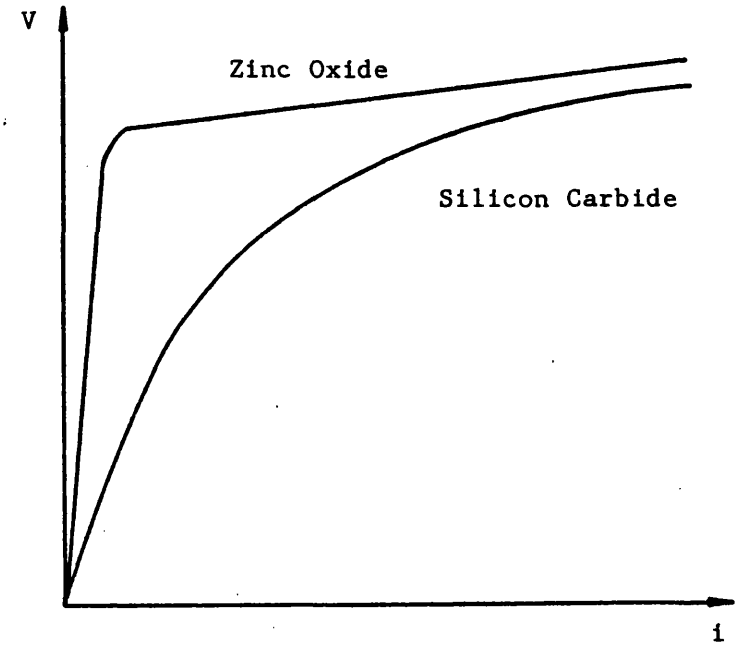


Fig 3.6 Non-linear resistor characteristics

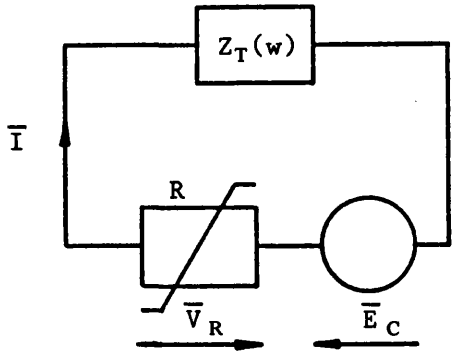


Fig 3.7 Thevenin equivalent circuit (frequency domain) for DGNS by-passing

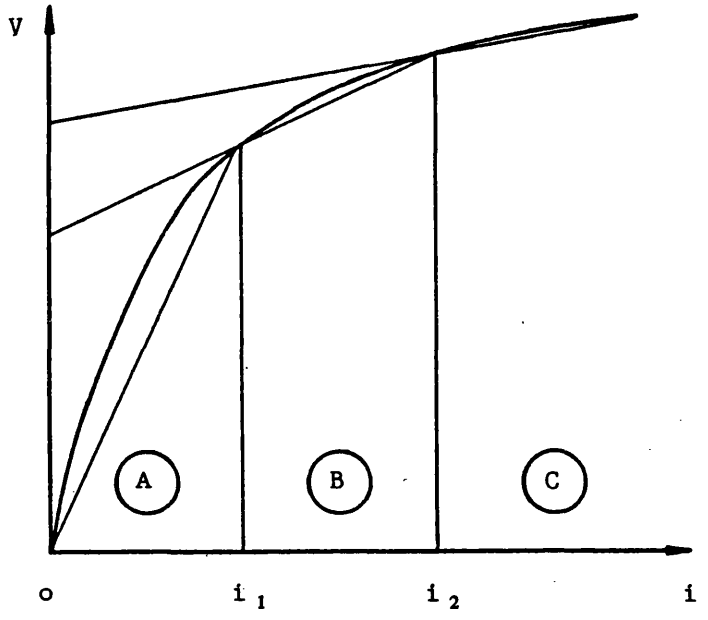


Fig 3.8 Piecewise linearisation of non-linear resistor characteristic

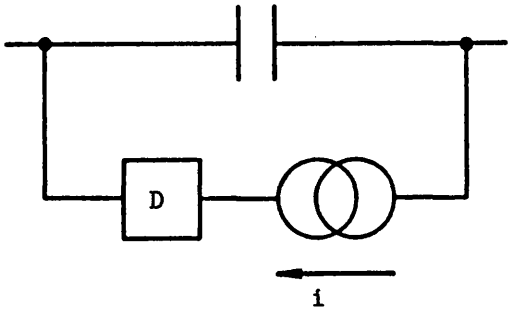


Fig 3.9 Capacitor reinsertion model

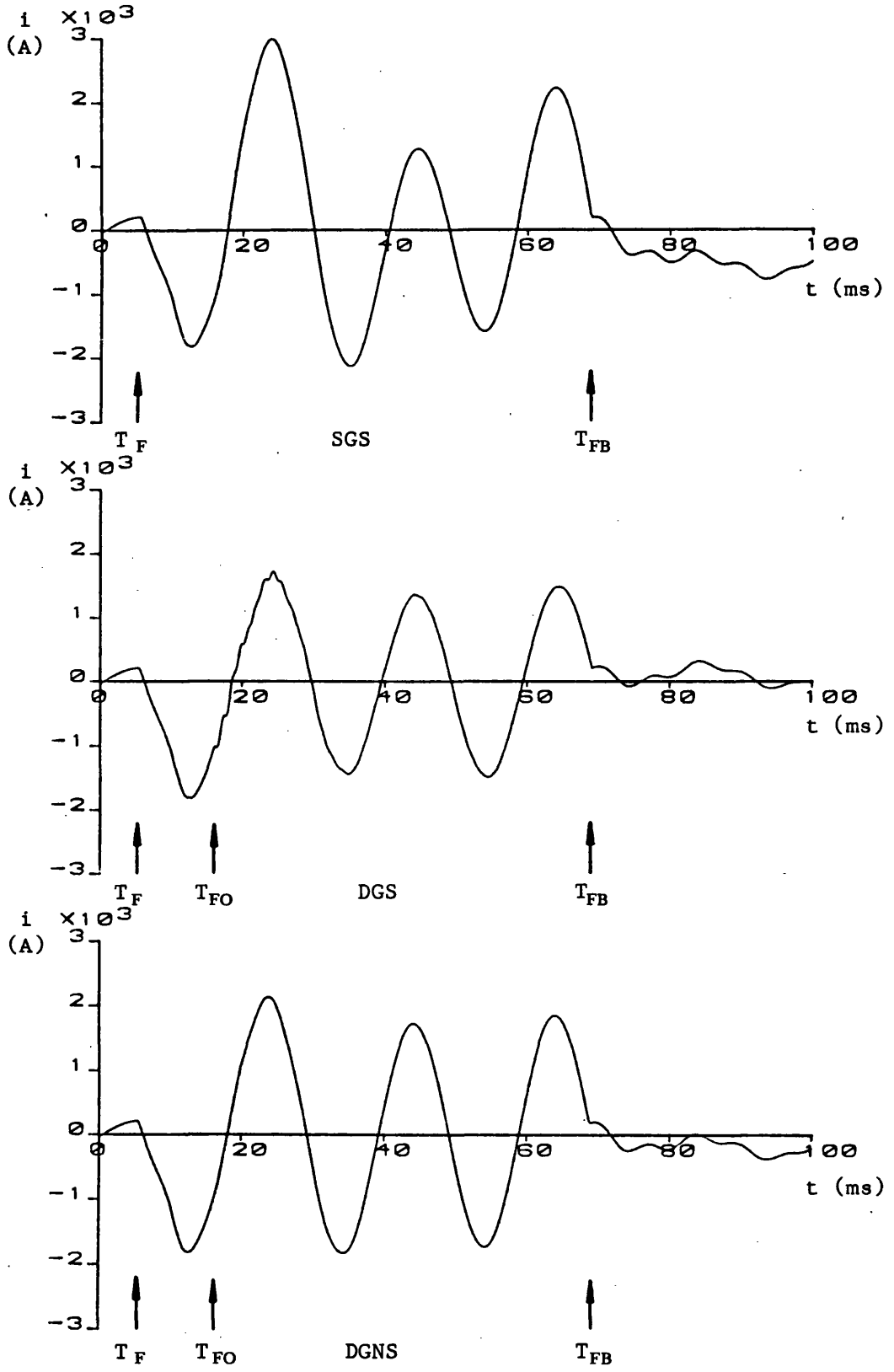


Fig 3.10 Faulted phase line currents for an 'a' to earth fault at 0° fault inception angle, no prefault power transfer

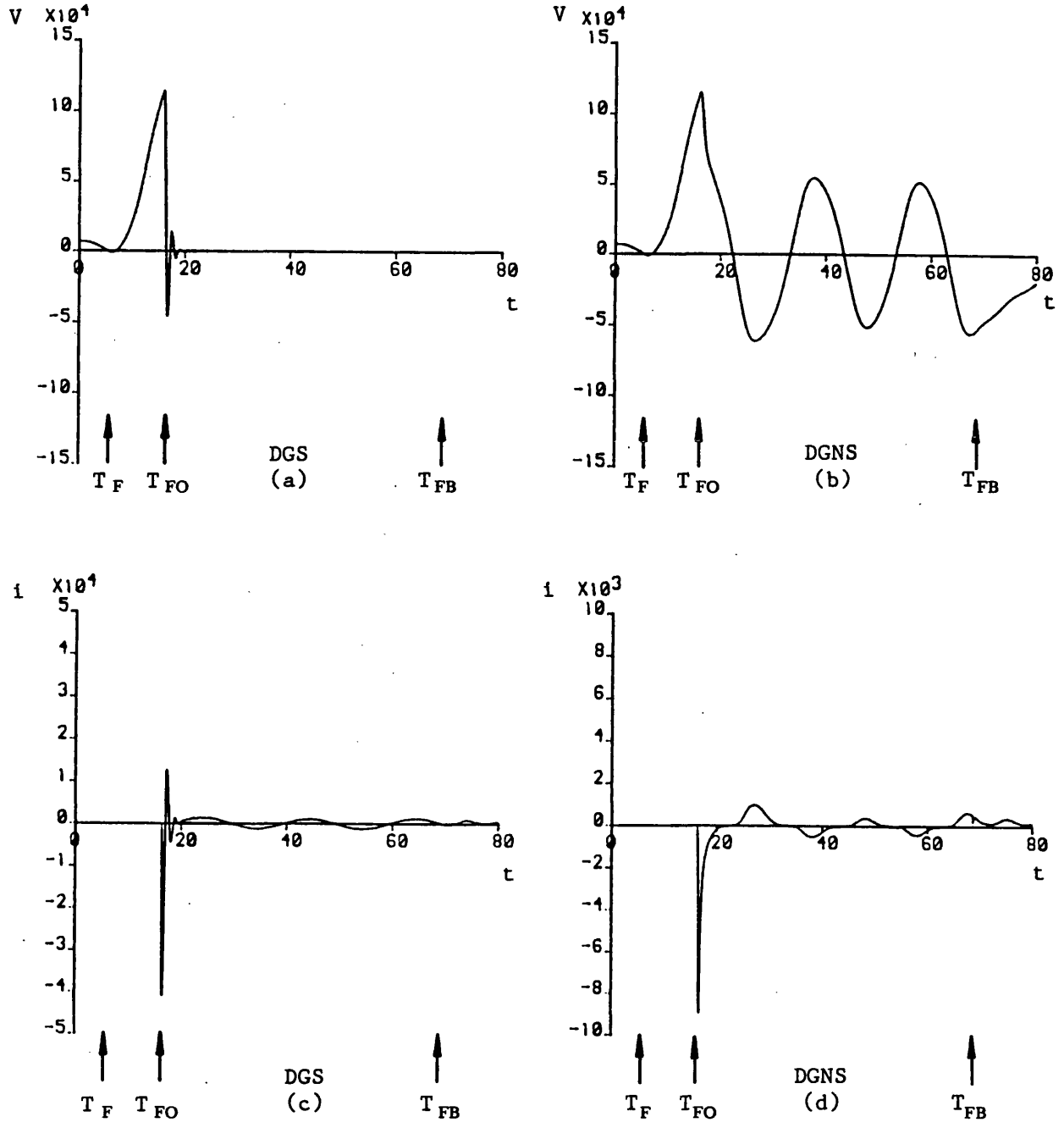
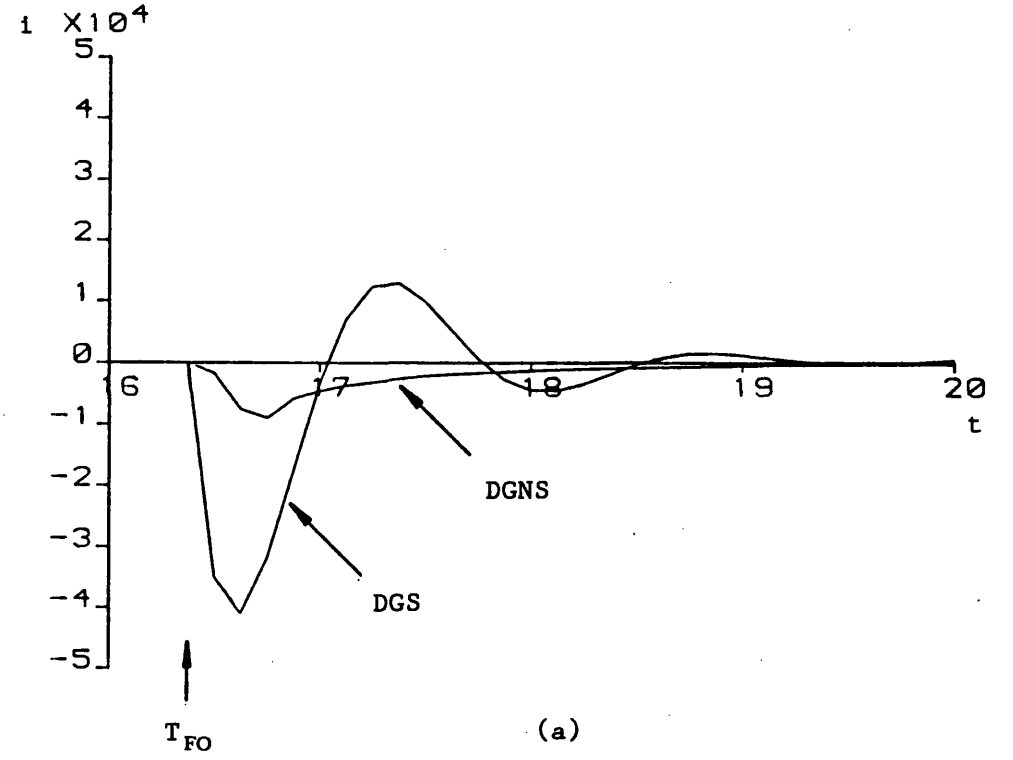


Fig 3.11 Waveforms for capacitor bank near busbar P showing comparisons between the DGS and DGNS

(a) 'a' phase capacitor voltage, DGS
(b) 'a' phase capacitor voltage, DGNS
(c) 'a' phase capacitor gap branch current, DGS
(d) 'a' phase capacitor gap branch current, DGNS



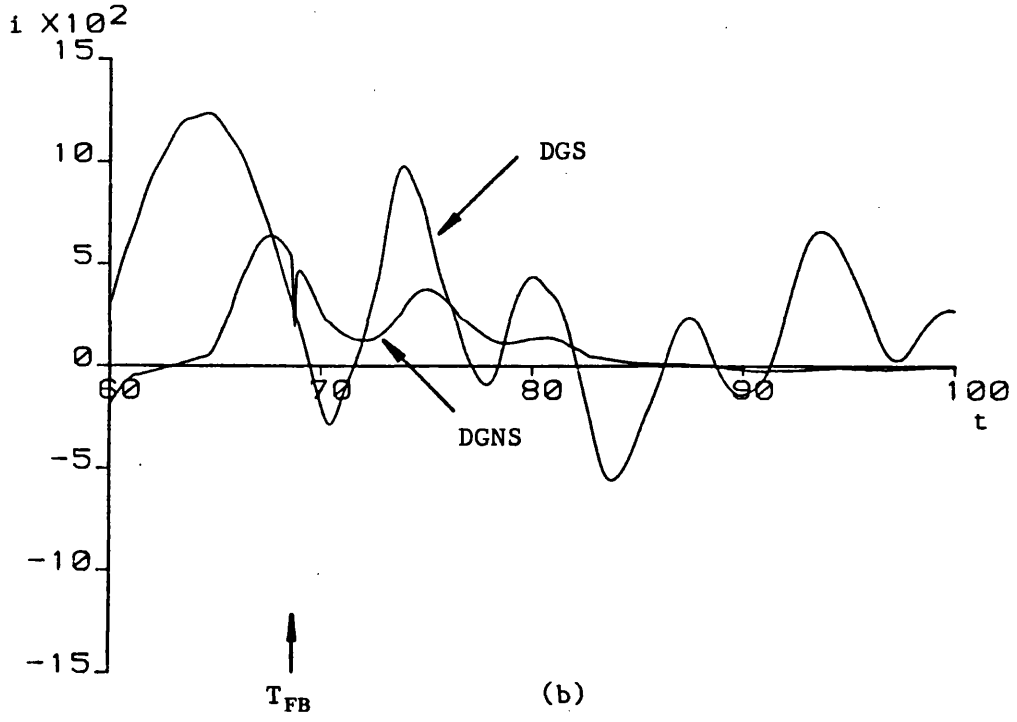


Fig 3.12 Detailed comparison of gap branch currents for DGS and DGNS following (a) gap flashover and (b) fault clearance

CHAPTER 4: DIRECTIONAL RELAYING PRINCIPLES

The analysis of system faults in terms of superimposed voltage and current components has been described in previous Chapters. Any relaying scheme based upon such measurands is fundamentally sound since the latter are informative of the transient condition alone. Furthermore, relaying signals comprised of modal superimposed voltage and current components offer the distinct advantages, in terms of security, over relays employing segregated phase comparisons, as outlined in Chapter 2. The proposed relaying scheme is fundamentally based upon the modal superimposed quantities, but to aid comprehension of the fundamental operating principles, the bulk of the analysis refers to a single conductor system which is therefore devoid of complications due to interphase coupling.

4.1 Direction Fault Detection

4.1.1 Surge Propagation

A single conductor system, linking two ends P and Q is shown in Fig 4.1. The latter includes the positions of two directional relays forming the proposed unit line protection scheme and the specified directions of current are important to the understanding of the basic operating principle. The de-energised network corresponding to the above system is thus drawn in Fig 4.2, where the line sections are represented by surge impedances, such that;

$$Z_o(w) = \frac{R(w) + jwL(w)}{G(w) + jwC(w)} \qquad \text{--- 4.1}$$

Where R, G, L, C are the distributed parameters of the line section. Now given that wL (w) >> R(w) and wC(w) >> G(w), in other words virtually lossless transmission, and that the parameters can, for simplicity, be considered frequency independent, then $Z_O(w)$ becomes real, such that;

$$Z_O = \sqrt{L/C} \qquad \text{--- 4.2}$$

Thus with respect to Fig 4.2, the sudden excitation of the system at F, by the application of the forcing V_F, causes the superimposed voltage wave to propagate towards each end with corresponding current components;

$$I_1 = I_2 = V_F/Z_O \qquad \text{--- 4.3}$$

Hence the voltage and current components at any point along the line are related by the line surge impedance Z_O, with the velocity of propagation being;

$$c = \sqrt{LC} \simeq 3 \times 10^8 \text{ m/s (lossless line)} \qquad \text{--- 4.4}$$

From basic transmission line theory, it is well known that points of impedance discontinuity presented to incident waves, cause partial reflections of the latter. Series capacitors therefore, offering an immediate step impedance change, may influence any travelling wave component passing through them. The series capacitors are always in circuit during the initial post-fault period and the simplified equivalent circuit of Fig 4.3, showing only the capacitor/line section from F to Q, is used to determine the influence upon the incident waves. Assuming an infinite bus at Q for simplicity, an equivalent terminating impedance presented to point A is thus;

$$Z_T = Z_C + Z_O \qquad \text{--- 4.5}$$

Hence, a wave V_F, propagating from F through Z_O will undergo the following reflection;

$$V_R = \frac{(Z_T - Z_O).V_F}{Z_T + Z_O}, \qquad \text{--- 4.6}$$

with the associated transmitted component being;

$$V_T = \frac{(2.Z_T).V_F}{Z_T + Z_O} \qquad \text{--- 4.7}$$

Now since the current through a previously uncharged capacitor (de-energised network) is limited only by the impedance associated with the applied voltage source and the initial impedance of the capacitor may be taken as zero. In other words, the voltage across the capacitor cannot be changed instantaneously, hence Z_C is assumed to be zero. Therefore the foregoing equations become;

$$Z_T = Z_O$$

$$\text{and} \quad V_R = 0 \qquad \text{--- 4.8}$$

$$V_T = V_F$$

Thus the propagation of the surges in the initial period subsequent to fault inception may be analysed as if the circuit were uncompensated.

4.2 Relaying Signals

Any fault occurring in between the two ends is referred to as internal or forward to both relays. Conversely, a fault behind either relay is considered as external, that is forward to one relay and reverse to the other. Since two directions to fault are possible it is then necessary to formulate two relaying signals, which for the proposed scheme take the familiar form [15];

$$S_1(t) = V(t) + I(t).R_O$$
$$S_2(t) = V(t) - I(t).R_O \qquad \text{--- 4.9}$$

Where V(t), I(t) are the superimposed voltage and current components measured at the relay location, and R_O is a replica resistance, matched to the surge impedance of the line, Z_O, the importance of which will become clear later. The behaviour of the two signals under both internal and external fault conditions is explained below.

4.2.1 Internal Fault

For the de-energised network of Fig 4.2, the application of the fault point generator causes the propagation of the voltage and current waves, and subsequent reflections, to form the lattice diagram of Fig 4.4. The latter assumes constant reflection coefficients at the source terminations and no resistance in the fault path. Hence the relevant voltage reflection coefficients are as follows;

$$k_{VP} = (Z_P - Z_O)/(Z_P + Z_O)$$
$$k_{VQ} = (Z_Q - Z_O)/(Z_Q + Z_O) \qquad \text{--- 4.10}$$

and $k_{VF} = -1$ (effectively isolating the two sections, P to F and F to Q)

Since the propagation velocity is approximately 3 x 10^8 m/s, there is a finite delay before the components reach the relay locations, given by;

$$T_{PF} = \sqrt{LC} \times x_{PF} \text{ and } T_{PQ} = \sqrt{LC} \times x_{FQ} \quad \text{--- 4.11}$$

From the lattice diagram, the total voltage and current variations at either end are found from the summation of each wave component and for end P in particular;

$$V_P(t) = [1+k_{VP}].V_F(t-T_{PF}) - k_P[1+k_{VP}].V_F(t-3T_{PF}) \quad \text{--- 4.12}$$

and for the current, taking into account the specified direction of current measurement;

$$I_P(t) = \frac{[k_{VP}-1].V_F(t-T_{PF}) + k_P[1-k_{VP}].V_F(t-3T_{PF})}{Z_O} \quad \text{--- 4.13}$$

Thus for $T_{PF} < t < 3T_{PF}$;

$$V_P(t) = [1+k_{VP}].V_F(t) \text{ and } I_P(t) = [k_{VP}-1].V_F(t)/Z_O \quad \text{--- 4.14}$$

The relaying signals are then;

$$S_1(t) = [1+k_{VP}].V_F(t) + ([k_{VP}-1].V_F(t)/Z_O).R_O \quad \text{--- 4.15}$$

and $S_2(t) = [1+k_{VP}].V_F(t) - ([k_{VP}-1].V_F(t)/Z_O).R_O$

If the replica resistance is matched to the surge impedance Z_O then;

$$S_1(t) = 2.k_{VP}.V_F(t)$$

and $S_2(t) = 2.V_F(t)$

ie $$\underline{S_1(t) = k_{VP}.S_2(t)} \quad \text{--- 4.16}$$

For time t just greater than $3T_{PF}$;

$$V_P(t) = [1-k_{VP}^2].V_F(t) \qquad \text{--- 4.17}$$

and $I_P(t) = [2k_{VP}-k_{VP}^2-1].V_F(t)/Z_O$

thus $S_1(t) = 2k_{VP}.[1-k_{VP}].V_F(t)$

and $S_2(t) = 2.[1-k_{VP}].V_F(t)$

ie $\underline{S_1(t) = k_{VP}.S_2(t)}$ --- 4.18

For all real systems, the range of values that the reflection coefficient k_{VP} can take is $-1 < k_{VP} < 1$, hence for all time subsequent to fault inception, the magnitude of S_1 is always less than S_2, ie $|S_2| > |S_1|$.

4.2.2 External Fault

The de-energised network of Fig 4.5 shows a fault location just behind busbar P, which causes a voltage and hence a current wave to propagate towards Q.A similar lattice diagram to the case above is constructed as in Fig 4.6, with the total variations at P given by;

$$V_P(t) = V_F(t) \qquad \text{--- 4.19}$$

and $I_P(t) = [V_F(t) - 2.k_{VQ}.V_F(t-2T) + 2.k_{VQ}^2.V_F(t-4T)]/Z_O$

where T is the transit time from P to Q. Hence for $0 < t < 2T$;

$$V_P(t) = V_F(t) \qquad \text{--- 4.20}$$

and $I_P(t) = V_F(t)/Z_O$

The relaying signals formed from these components then become;

$$S_1(t) = 2V_F(t) \text{ and } S_2(t) = 0 \qquad \text{--- 4.21}$$

ie $|S_1| > |S_2|$.

Thus the opposite effect of the magnitude of S_1 being larger than S_2, in the initial period, is observed. However, considering the subsequent period $2T < t < 4T$, the following relations are available;

$$S_1(t) = 2.[1-k_{VQ}].V_F(t) \qquad \text{--- 4.22}$$

and $S_2(t) = 2.k_{VQ}.V_F(t)$

thus $S_1(t) = ([1-k_{VQ}]/k_{VQ}).S_2(t) \qquad \text{--- 4.23}$

For $-1 < k_{VQ} < +1$, Eq 4.23 reveals that the arrival of the components reflected at Q, at time $t = 2T$, may cause the initial magnitude relationship of S_1 and S_2 to be reversed, ie the magnitude of S_2 may be larger than that of S_1 for this external fault condition. After a further period of 2T seconds however, the original magnitude relationship is restored by the arrival of further reflected components, with the signal ratio being as follows;

$$S_1(t) = -(1/[k_{VQ}^2-k_{VQ}] + 1).S_2(t) \qquad \text{--- 4.24}$$

and for $-1 < k_{VQ} < 1$, there is no value of k_{VQ} which satisfies the expression $|S_1| < |S_2|$.

In summary, the foregoing analysis has shown that the initial variations of the superimposed voltage and current components are such that the relaying signals provide a suitable criteria for determining the direction to fault, that is;

$|S_2(t)| > |S_1(t)|$ indicates a forward fault --- 4.25

and $|S_1(t)| > |S_2(t)|$ indicates a reverse fault.

The former relation is valid for all time after the arrival of the superimposed components at the relaying point, whereas the latter is

always valid initially, but subsequently, is subject to staggered time periods of correct and incorrect indication. To this end, special filtering techniques have been developed, as described in Chapter 5, to emphasise the lower frequency signal behaviour and hence to increase the security of the directional decision, in the presence of high frequency travelling waves.

The analysis has been carried out assuming solid fault conditions, but the inclusion of some finite fault path resistance merely alters the waveshape of the forcing voltage. Additional components reflected from each end may then be partially transmitted through the fault point, thus affecting the variations at the other end, but the directional properties of the components and hence the established magnitude criteria remain unchanged. Moreover, a resistive fault path tends to reduce the probability of magnitude relationship reversal for the reverse fault condition, since the incident wave is then only modified by the fault/source termination, instead of being totally reflected and inverted.

4.3 Effects of Remote Infeeding Generation

The source termination considered above are representative of a single machine providing all of the infeed at the busbars. However, multisection systems comprising plain and compensated feeders, are widely encountered in the working environment. In such situations the remote generation and infeeding line sections may, for the purpose of fault transient analysis, be modelled into composite equivalents, which then reduces the network to something similar to the simple interconnection of Fig 4.1. However, any surge components

which propagate towards the remote ends, would be partially reflected and hence return as incident waves to the relaying location. For the de-energised system of Fig 4.7, the lattice diagram of Fig 4.8 illustrates the surge pattern for the situation in which $x_{PF} > x_{RP}$. Again the assumptions are made that $k_{VF} = -1$ (solid fault) and that k_{VP} and k_{VR} are constant. If T_1 is the transit delay from P to F and T_2 is the transit time from P to R, the voltage and current variations for $T_1 > T_2$, are described by;

$$V_P(t) = (1 + k_{VP})V_F(t - T_1) + (1 + k_{VP})^2 k_{VP} V_F(t(T_1 + 2T_2))$$

and $$I_P(t) = [(k_{VP} - 1) V_F(t - T_1) + (1 + k_{VP})^2 k_{VR} V_F(t-(T_1 + 2T_2))]/Z_O$$

For time t just greater than T_1 ;

$$S_1(t) = 2k_{VP}V_F(t) \text{ and } S_2(t) = 2V_F(t)$$

hence $|S_2| > |S_1|$ as required. However, for time t just greater than $T_1 + 2T_2$;

$$S_1(t) = 2(k_{VP} + (1 + k_{VP})^2 k_{VR}).V_F(t) \text{ and } S_2(t) = 2V_F(t)$$

Therefore, if the condition $k_{VP} + (1+k_{VP})^2 k_{VR} > 1$ is satisfied, then $|S_1| > |S_2|$ for a forward fault.

Thus although the initial signal variations are always consistent with the developed magnitude criteria, there can be dependent upon the system configuration, a reversal of the initial directional indication. Thus the enhancement of the lower frequency signal behaviour, as achieved with the aforementioned filtering techniques is imperative for guaranteeing absolute security of decision for any arbitrary system configuration.

4.4 Effects of Variant Reflection Coefficients

Hitherto, the terminations behind the relays have been expressed in terms of constant surge impedances which therefore exhibit constant reflection coefficients. In practice of course, the source terminations are comprised of inductance and resistance and as such absorb and dissipate energy supplied by the forcing quantity, subsequently returning part of that energy to the latter. Such behaviour is dominant just beyond the initial surge condition and is particularly relevant for low frequency signals derived from narrow bandwidth transducers such as cvts. For the specific case of a fault close to a source termination, assuming for simplicity that the other end of the line section is perfectly matched, a simple de-energised circuit may be drawn as in Fig 4.9. The sudden application of the voltage source, $V_F(t)$, at the fault point, then generates the following variations;

$$V_F(t) = V_M.\sin(w_O t+\theta) \qquad \text{--- 4.28}$$

$$i_S(t) = V_M/Z_S.[\sin(w_O t+\theta-\psi) - \sin(\theta-\psi)e^{-t/T}]$$

where $Z_S^2 = R^2 + (w_O L)^2$

$\psi = \tan^{-1}(w_O L/R)$

and $T = L/R$

Similarly, expressions may be derived for effective capacitive/resistive terminations which may arise from double circuit feed rounds [10];

$$i_S(t) = V_M/Z_S.[\cos(wt+\theta-\psi) + a/w.\sin(\theta-\psi).e^{-at}] \qquad \text{--- 4.29}$$

where $Zs^2 = R^2 + (1/w_O C)^2$

$a = 1/RC$

$\psi = \tan^{-1}(w_O CR)$

The behaviour of the current, $i_S(t)$, described by Eqs 4.28 and 4.29, is characteristic of an offset sinusoid and for the inductive termination, the first zerocrossing of the voltage, after fault inception, causes the initial polarity relationship between the superimposed voltage and current to reverse. The result of this is that the signal magnitude criteria would then indicate the opposite direction to fault. Conversely, it is the first zerocrossing of the current associated with the capacitive termination which determines the polarity reversal instant. In both cases, the initial polarity relationships are regained shortly after this reversal period, hence the overall variation may be described in three time periods, as indicated by Fig 4.10. The voltage and current components upto time T_1 produce the correct magnitude relationship between S_1 and S_2, ie $|S_2| > |S_1|$ for a forward fault. After the period T_1 , ie $T_1 < t < T_2$, the voltage and current components are incorrectly indicative of the direction to fault, but clearly, this period is relatively small when compared to the total period $T_1 + T_3$ during which correct indication is available.

At this stage it is worth emphasising that the polarities of the voltage and current components are independent of their relative magnitudes. This in turn ensures that the directional magnitude criteria applied to the relaying signals, remains valid under conditions where the signals are dominated by either the voltage of current component. Thus with respect to the original signal expressions of Eq 4.9, it is not essential for the product $I(t).R_O$ to be equal in magnitude to $V(t)$, and as such perfect matching of R_O to the line surge impedance, which of course in practice, is virtually impossible, is no longer a necessity.

For the inductive termination, the period T_1 is 10, 5 and 2.5 ms for fault angles of 0,90 and 135° respectively with a 50 Hz forcing voltage. It may be shown that regardless of the fault angle or X/R ratio of the source, the voltage and current components have the correct relative polarity during period T_1. Some degree of difficulty exists however when analysing the capacitive termination, since it is the current component and not the well defined forcing voltage which determines the period T_1. For a purely capacitive termination ($X_C \gg R$), the superimposed components are indicative of the opposite direction to fault. However, no such situation is possible in practice because the presence of any finite resistance biasses the current towards the correct polarity with respect to the applied voltage. Such behaviour is nothing more than the standard transient condition of a resistor/capacitor charging arrangement. As correctly pointed out in Reference 10, the steady state transient condition may cause the source behind the relaying point to appear capacitive (making the extreme assumption of negligible source and line resistance), but the new scheme is in fact designed to operate on the total superimposed component, particularly in the initial post fault period. Thus the straightforward assumption that the source may be represented by pure capacitance is not in fact the correct way to analyse the behaviour of the proposed directional scheme. The conclusion is that regardless of the nature of the reactive component behind the relay, the presence of any finite resistance enables the reliable determination of the direction to fault to be gained from the initial signal variations.

4.5 Multiphase Directional Relaying

With the adoption of the modal decoupling technique, the behaviour of a multiphase system may be described in terms of 'n' separate single phase type circuits, where 'n' is the number of phases involved. This technique is successfully applied to transmission lines and the assumption of ideal transposition of conductors, throughout the entire length of the line section, leads to a frequency invariant modal transformation matrix [S]. The latter, in conjunction with it's inverse, diagonalises the system matrix [P] where [P] is formed from the product of the series impedance and shunt admittance matrices of the system, and there are an infinite number of matrices which are able to perform such a task. By careful choice of the matrix [S], scalar elements are found such that $[S][P][S]^{-1}$ is diagonal. The benefits of a scalar transformation are two fold;

a) The theoretical analysis of the transient behaviour of the systems is very much simplified.

b) For digital computation, the extra time and memory requirements associated with complex arithmetic are removed.

One such matrix, known as the Karrenbauer transformation matrix takes the form;

$$[S] = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & -2 \\ 1 & -2 & 1 \end{bmatrix} \quad \text{and} \quad [S]^{-1} = 1/3 \begin{bmatrix} 1 & 1 & 1 \\ 1 & 0 & -1 \\ 1 & -1 & 0 \end{bmatrix}$$

Therefore consideration of the established relationship between the modal and phase voltages, $[V_C] = [S]^{-1}[V]$ gives;

$$V_{C1} = (V_A + V_B + V_C)/3$$

$$V_{C2} = (V_A - V_C)/3 \qquad \text{--- 4.30}$$

and $$V_{C3} = (V_A - V_B)/3$$

The Aerial mode components (modes 2 and 3) exhibit the same propagation characteristics ie $Z_{02} = Z_{03}$ and $c_2 = c_3$, and consideration of Eq 4.30 suggests that for all types of fault, either one or both of the Aerial modes is excited, regardless of the Earth mode. The latter enables the processing of only the Aerial modes for relaying purposes, thereby reducing signal processing requirements, without loss of discrimination for all fault types. A further significance of utilising only the Aerial mode quantities is that unlike the Earth mode, the superimposed currents circulate within the boundary of the Aerial path without the need for an earth return. When considering double circuit applications therefore, independent relaying of each circuit is made possible, since the Aerial current distributions summates to zero, effectively isolating or de-coupling the two circuits.

The relaying signals of Eq 4.9 are thus formed for each mode;

$$S_1(t)_{2,3} = V(t)_{2,3} + I(t)_{2,3} \cdot R_O$$

and $$S_2(t)_{2,3} = V(t)_{2,3} - I(t)_{2,3} \cdot R_O$$

Where $V(t)_{2,3}$ and $I(t)_{2,3}$ are the mode 2 and 3 superimposed voltage and current components respectively.

The behaviour of the modal relaying signals in terms of directional magnitude relationships, for both forward and reverse faults is somewhat similar to the single phase case. The problems encountered

with segregated phase relaying schemes, associated with sound or healthy phase coupling are overcome, since the behaviour of any particular modal signal is independent to, and hence has no effect upon, the other two modes. For any type of fault, the three phase system condition is represented by three interconnected modal circuits, a technique similar to that of symmetrical components. The Aerial mode impedances are akin to those of the pps quantities with the distinct advantage that the modal analysis is valid from the very instant of fault inception, whereas the symmetrical component technique is only valid under steady state conditions. Thus the modal components utilised by the new relaying scheme enable the latter to render a reliable decision with the minimal degree of post fault delay.

For all types of fault, Reference 20 describes the modal circuit interconnections which enable the relaying point quantities to be estimated for verification of the foregoing magnitude criteria. Only three phase solid faults are seen to produce total reflection at the fault point ($k_{VF} = -1$), whilst for all other fault types, partial transmission of components through the fault point is possible. Thus the magnitudes of the superimposed components produced at each end are affected by the source and line impedances at the opposite ends. However, as described earlier, the initial signal variations are such that the directional criteria is in no way affected.

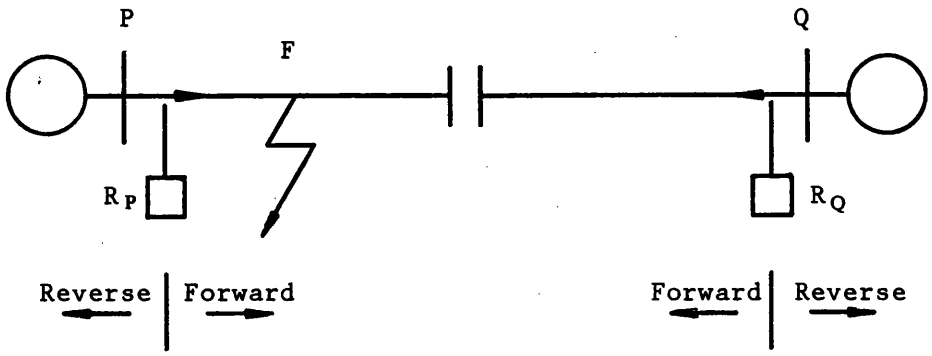


Fig 4.1 Single conductor system with directional relays R_P, R_Q

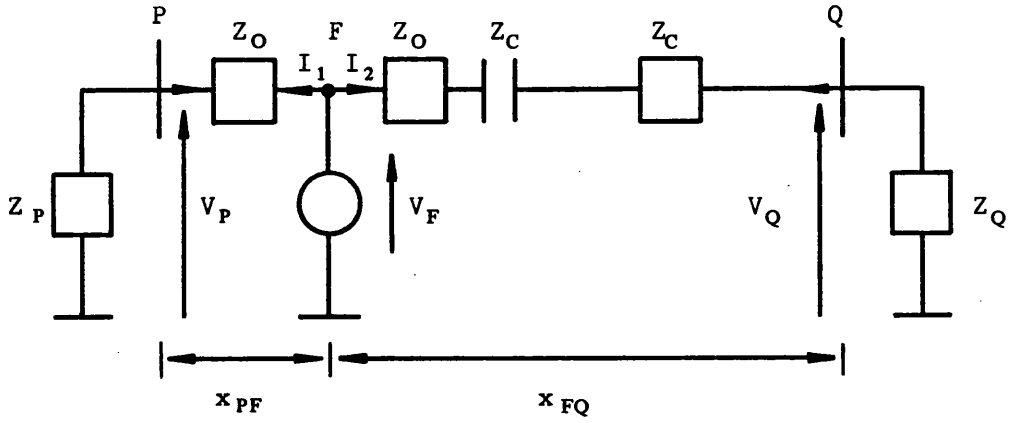


Fig 4.2 De-energised network for system of Fig 4.1

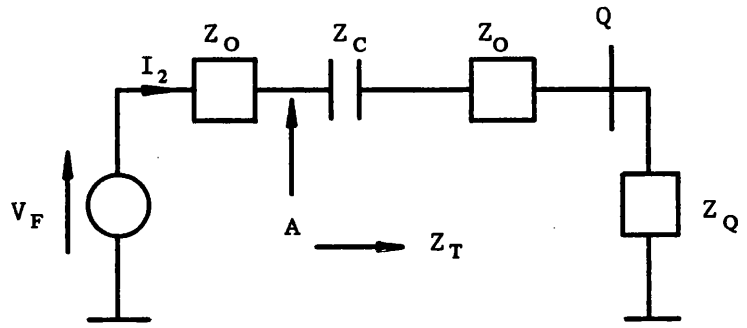


Fig 4.3 Equivalent circuit from fault point to end Q

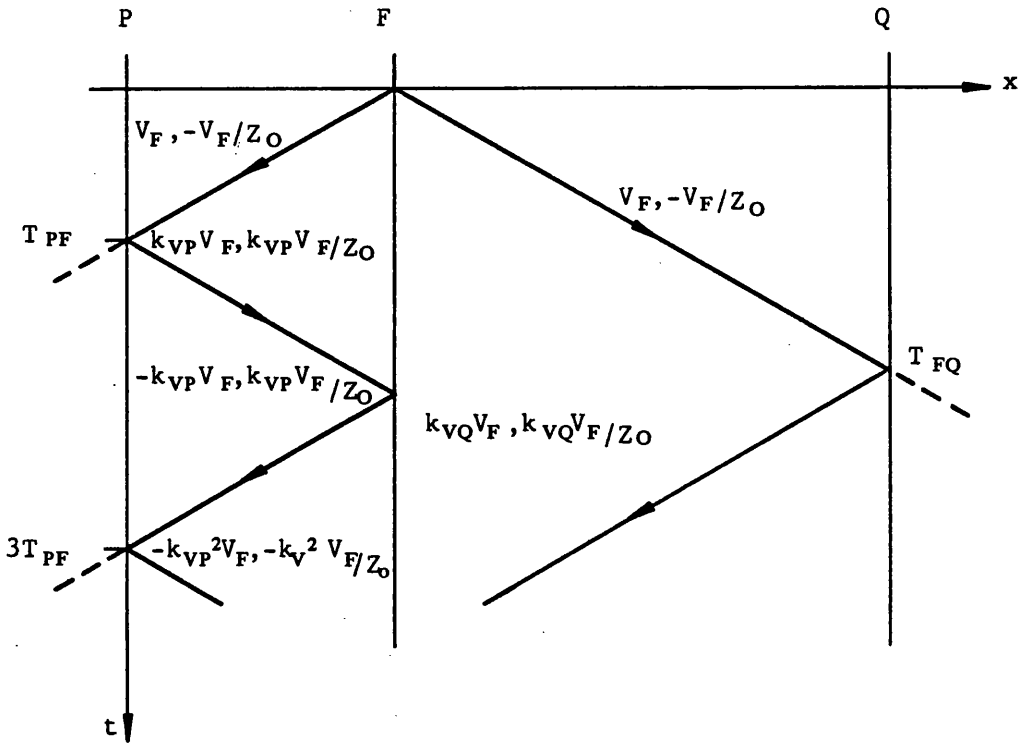


Fig 4.4 Lattice diagram for internal fault condition of Fig 4.2

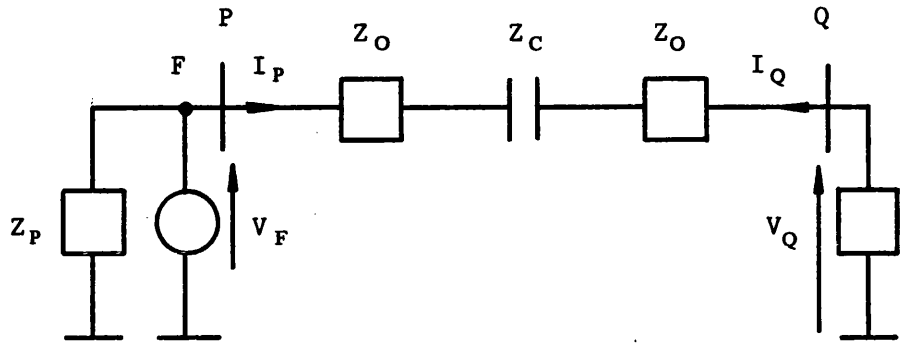


Fig 4.5 De-energised network for external fault on single conductor system

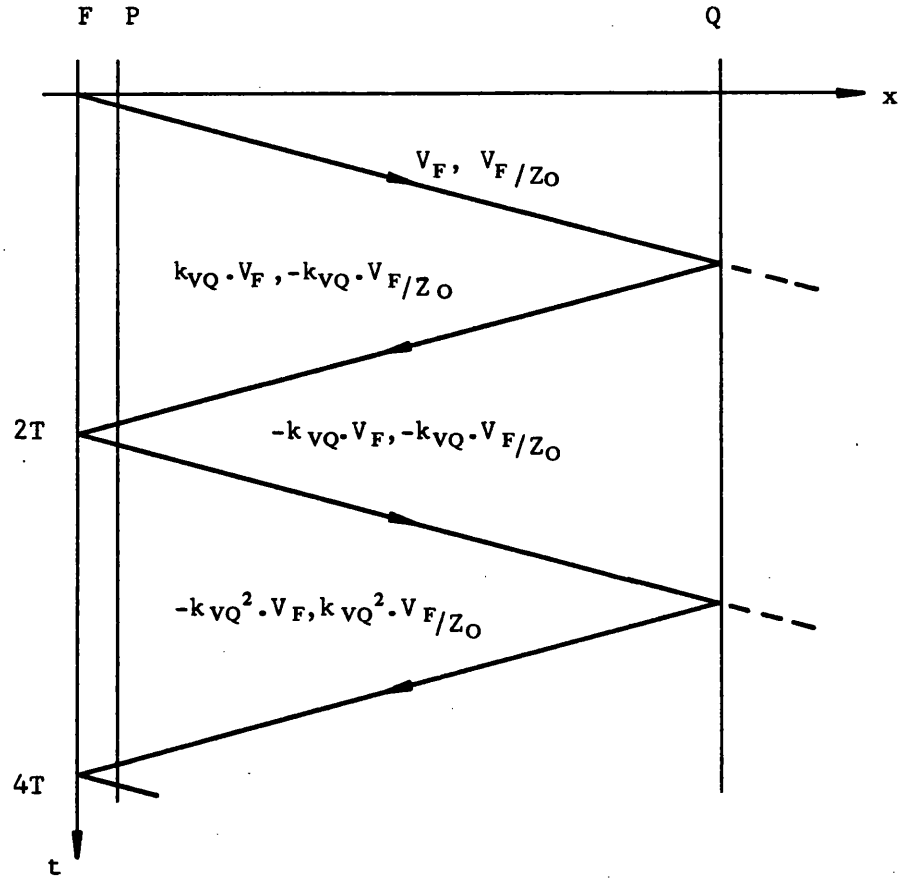


Fig 4.6 Lattice diagram for external fault condition of Fig 4.5

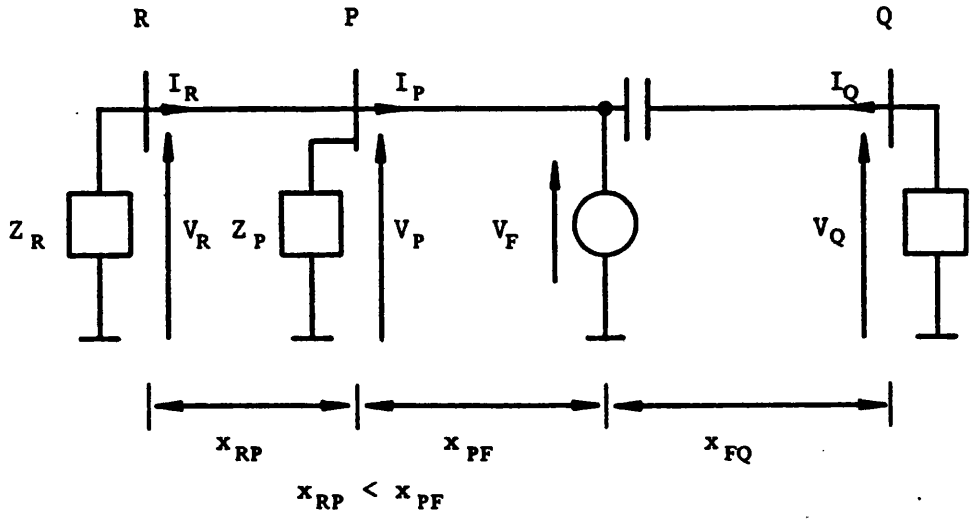


Fig 4.7 De-energised network with infeeding line section R-P, internal fault

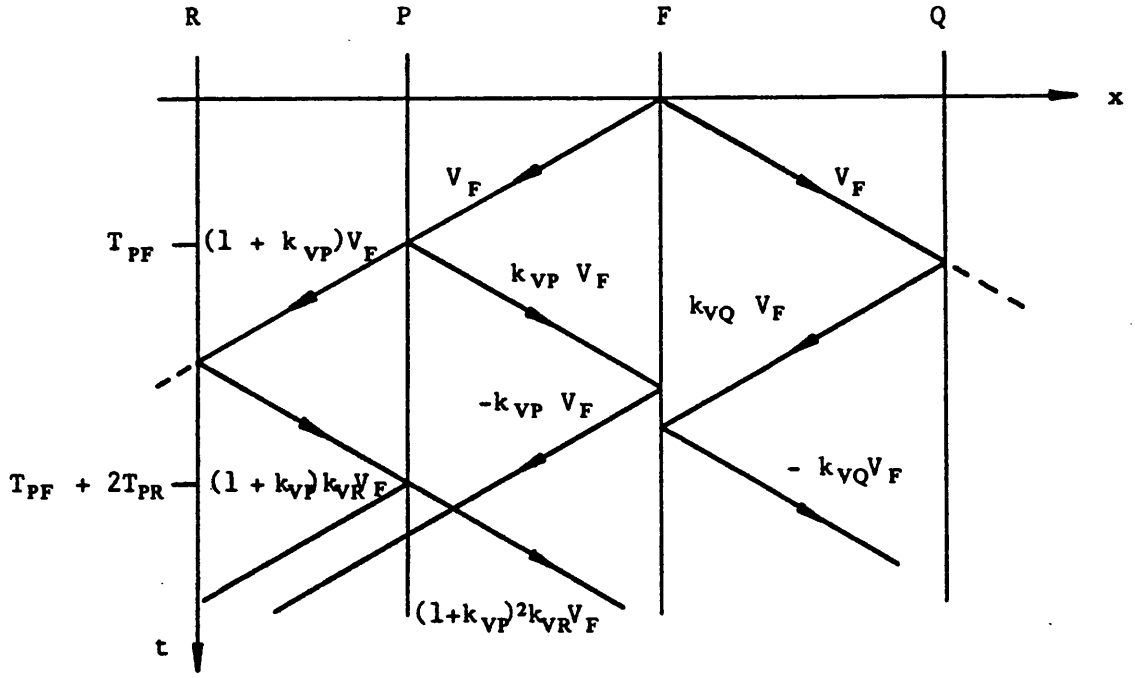


Fig 4.8 Lattice diagram for fault condition in Fig 4.7, showing voltage component reflections only

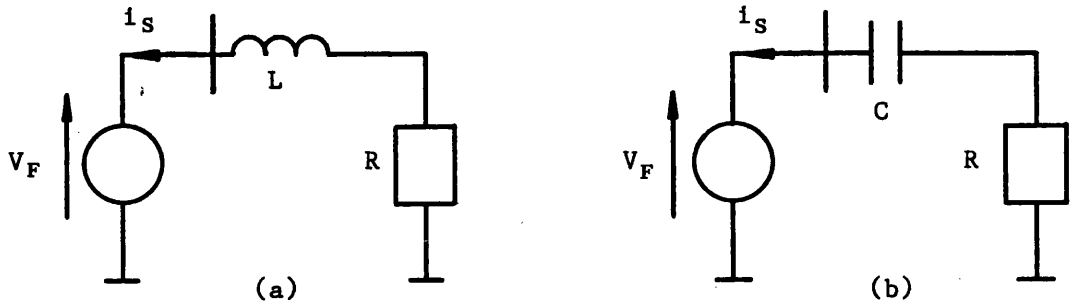


Fig 4.9 Inductive and capacitive source terminations

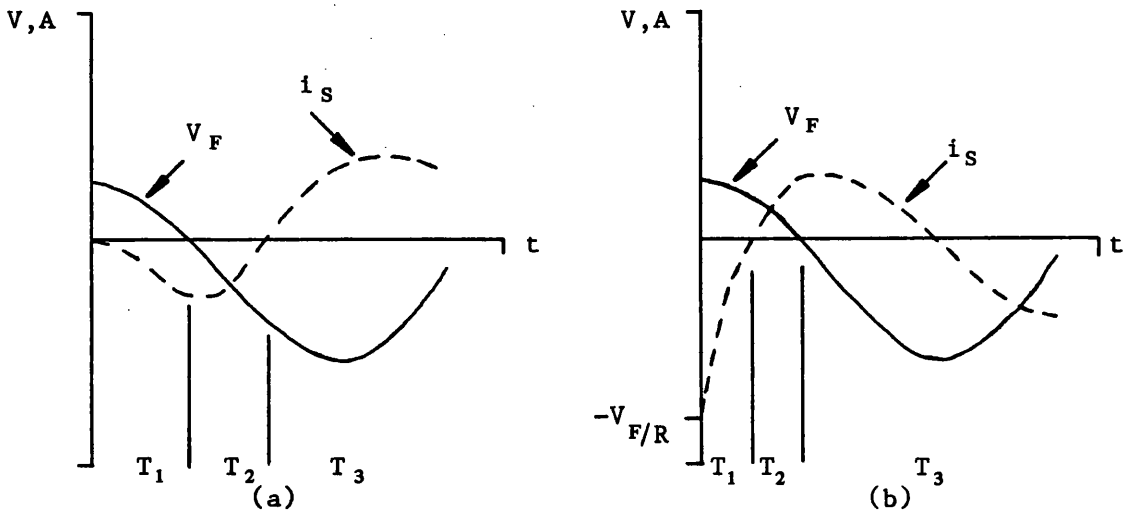


Fig 4.10 Superimposed voltage and current variations for inductive and capacitive source terminations

CHAPTER 5: COMPUTER IMPLEMENTATION OF DIRECTIONAL RELAY

The proposed relay is designed for implementation with the latest generation of 16 bit microprocessors, which together with the analogue pre-filters, forms a hybrid scheme. In computer simulation terms, the difference in analogue and digital quantities is only that the former is performed with floating point arithmetic, and the latter with integers. The total variations of secondary voltage and current are mixed into modal form at the analogue stage, to form the two Aerial mode components alone. The advantage of this is that the number of A/D conversions is reduced from 6 (three voltages and currents) to 4, with obvious savings in conversion times.

The signal processing and decision making are performed digitally for the following reasons;

a) The superimposed quantities are extracted from the total variations with no delay, which cannot be reliably achieved with analogue steady state suppression devices. The alternative in analogue form is to use charge coupled devices, but these have a history of poor in circuit performance and are often subject to irregular outputs arising from clock synchronisation problems.

b) Algorithm and constant changes as required for different system applications are effected simply by software re-programming. Such changes in analogue form would constitute device replacement.

c) Microprocessors are inherently suitable for self checking or testing which is an attraction from a commercial point of view, since this directly contributes to the availability of the relaying scheme as a whole.

d) Minimal interfacing is required for modern digital communication systems, a factor of prime importance when two ended protection schemes are employed.

The block diagram, of the proposed scheme from the primary system, to the relay outputs is shown in Fig 5.1, each section of which is described below.

5.1 Primary System Information

The primary system fault transient information is derived via the frequency domain techniques described in Chapter 2. The digital simulation is run at 8 kHz, which therefore yields accurate information of upto 4 kHz. It is pointless extending this bandwidth since the cvts which are used almost without exception on ehv systems, have a very low cut off frequency of typically 600 Hz. Most cts however have a very wide bandwidth, upto 10 kHz, but as detailed below, an interface is used in the current channel to generate a proportional voltage over a specified frequency range, much less than 10 kHz. Moreover, an analogue low pass filter is employed to pre-condition the signals, with a cut off frequency well below 4 kHz, hence the requirement to provide very high frequency primary system information, above 4 kHz, is removed.

5.2 Analogue Stages

5.2.1 Primary System Interface (PSI)

The PSI comprises the cvt and ct transducers, a current input module (CIM) and pre-filters. Because of the wide bandwidth of the ct, a simple turns ratio factor alone is introduced to simulate the latter, this ratio being for most applications, 1200 : 1. The CIM is the device which converts the secondary current input to an appropriate voltage level over a limited frequency bandwidth. The cvt, CIM and pre-filters in addition to imposing gain adjustments, also modify the input voltages and currents by frequency filtering, with the non-uniform frequency response of the cvt derived from a model, as described in Reference 20. From a modelling point of view, the CIM and pre-filters have well defined transfer functions derived from their circuit elements, from which corresponding time domain impulse responses are obtained via inverse Fourier methods.

The effect of any frequency modifying function f(t), upon a time domain variation y(t), may be determined using convolution, such that;

$$y^1(t) = \int_0^t f(T).y(t-T)dT \qquad \text{--- 5.1}$$

Where $y^1(t)$ is the modified version of y(t) and T is the dummy variable of integration. If the time scale is divided into 'n' discrete samples of width ΔT, Eq 5.1 may be evaluated via simple numerical integration, which gives;

$$y^1(n) = \sum_{k=0}^{n} f(k).y(n-k).\Delta T \qquad \text{--- 5.2}$$

Hence, the primary voltages and currents at any sample 'n', are found using a past history of the relevant impulse response f(k), together with the profile of the input signal, for the cvt, CIM and pre-filters in turn. The cvt ratio for the simulation is taken as $110/500 \times 10^3$ for the 500 kV studies, whilst at power frequency, the CIM and pre-filter have unity gain.

5.2.2 CIM Transfer Function

A typical CIM, employed in conventional distance protection equipment, is as shown in Fig 5.2. This module has proven satisfactory in the working environment, and is found to be suitable for this application. The Laplace transfer function is given by;

$$T(s) = R3/R1)s.[s + (1/R4.C)]/[s + (1/(R2 + R4).C))] \text{ --- } 5.3$$

with the following component values;

R1 = 16 KΩ R2 = 1 KΩ

R3 = 5.66 MΩ R4 = 16 KΩ

C = 22 nF

The expression of Eq 5.3 is obtained assuming that the transactor acts as a pure differentiator, ie v = si. The above component values then yield an upper cut-off frequency of the CIM of 7.2 kHz. The

windings of the transactor however, suffer from interturn capacitance effects, which introduce a pole around 3.5 to 4 kHz, consequently reducing the bandwidth of the CIM. This effect is too complex for modelling purposes to be considered here, but as explained below, some pre-filtering is introduced and as such, no overall accuracy is lost by ignoring the interturn capacitance.

5.2.3 Analogue Pre-Filter

A second order low pass Butterworth filter is suggested for the hardware implementation of the pre-filter, the transfer function of which takes the standard form;

$$T(s) = w_n^2/(s^2 + 2\zeta w_n + w_n^2) \qquad \text{--- 5.4}$$

The choice of cut-off frequency w_n is largely dependent upon the digital stages of the relay. As stated previously, a 4 kHz bandwidth of information is available from the primary simulations, but in practical terms, an 8 kHz digital implementation required to interpret this information is too demanding with respect to duty cycle times for even the latest microprocessors. Such a sampling frequency would require that all operations on both signals S_1 and S_2, be completed within 1/8000 = 125 μs. Conversely, a much lower frequency reduces the rate of rise of the signals through the digital stages and obviously extends the decision rendering time scales. A compromise between speed and capacity is reached with the optimum sampling at 4 kHz, which when reciprocated, produces a rational time step ΔT. (At this point it is worth mentioning that for 60 Hz systems, the sampling frequencies of the primary and secondary

simulations are increased to 9.6 and 4.8 kHz respectively, in order that an integer number of samples are produced per power frequency cycle.)

For a secondary sampling rate of 4 kHz, the Nyquist frequency is thus 2 kHz, which then sets the cut-off frequency for the pre-filter. All components above 2 kHz, if unfiltered, would be mapped or translated down into the d.c. to 2 kHz spectrum by the digital process. This cut-off frequency is high enough for the pre-filter not to introduce any significant delay into the measurands. It should be noted that most types of protection equipment employ some degree of pre-filtering for noise suppression.

To illustrate the effects of the cvt and pre-filter, two fault conditions were simulated, one for an 'a' phase to earth fault at the relay location and the other for an interphase ('b' to 'c') fault not involving earth, 15 km away. The primary and secondary cvt responses to the former case are illustrated in Figs 5.3a and b, in which the cvt relaxation transient, which may persist for several cycles, is clearly evident. Fig 5.3c shows the primary system phase voltages for the interphase fault, clearly corrupted by very high frequency travelling waves. With the 2 kHz pre-filter, Fig 5.3d illustrates the severe attenuation of the latter, whilst the effect of the very low cut-off frequency of the cvt (@ 600 Hz) produces a marked contrast as seen in Fig 5.3e.

Realistic secondary waveforms have therefore been made available for testing purposes, and equipments for executing the above functions are seen to be similar to those currently employed in the field.

This should therefore make the new scheme attractive to those utilities well versed in standard protection gear.

5.2.4 Channel Gains k_v, k_i

In addition to the frequency filtering, the PSI incorporates two scalar adjustments, k_v and k_i, in the voltage and current channels respectively, to maximise the analogue signals to +/- 10 V peak. For the voltage channel, allowing for a primary overvoltage of 2 pu, and a 500 kV system, the maximum rms secondary line voltage is thus;

$$V = 2.500.10^3(110/500.10^3)$$

hence $V = 220$ volts --- 5.5

The corresponding peak phase voltage is therefore;

$$Vp = (1.414/1.732).220 = 179.6 \text{ volts} \quad \text{--- 5.6}$$

In order to limit this voltage to 10 V in the analogue section, a factor k_v is introduced, such that;

$$k_v = 10/Vp = 10/179.6$$

ie $\underline{k_v = 0.0557}$ --- 5.7

In the current channel, a factor k_i is introduced to limit the voltage equivalents of the phase current inputs to +/- 10 V. The choice of k_i depends entirely upon the setting philosophy adopted for the relay. The range of current levels encountered in integrated networks is extremely large and it is necessary to limit or clip the input current if the latter is very high. This permits a larger

gain for low current level faults, but introduces some degree of non-linearity into the process. The strategy adopted herein, for a directional comparison unit scheme, configured in a blocking mode, is that for internal faults, ultra fast relay recovery is not important, since breaker opening is initiated to clear the fault. However, maximum sensitivity of the relay should be recovered with minimal delay, which cannot be achieved with clipped input signals. Hence a current I_F is calculated as the maximum through or external fault current which may be measured at the relay location. Then allowing for some loading current I_L, the peak of the total current is scaled to 10 V, such that;

$$k_i = 10 / (1.414\ [I_F + I_L]) \qquad \text{--- 5.8}$$

5.2.5 Modal Mixing

With the adoption of the Karrenbauer modal transformation, the Aerial mode voltage components become;

$$V_2 = 1/3\ (V_a - V_c) \qquad \text{--- 5.9}$$

and $V_3 = 1/3\ (V_a - V_b)$

Under balanced three phase fault conditions, the input scaled phase voltages would therefore be 10 V in magnitude and for the mode 2 voltage in particular, Eq 5.9 becomes;

$V_2 = 1/3\ V_L$, where V_L is the line voltage V_{ac} .

thus $V_2 = 10/1.732$ --- 5.10

Hence to maintain the voltage (and current) levels at +/- 10 V after the modal mix, a factor km is introduced, such that $km.V_2 = 10$ V, hence km is simply equal to 1.732.

5.2.6 R_O Adjustment

The secondary surge impedance factor R_O, is accounted for prior to ADC, by introducing a further constant in the voltage channel, to provide the balance;

voltage channel gain = current channel gain/R_O

this is equivalent to multiplying the current component by R_O and in order to maintain a relatively high magnitude of analogue input voltage to the ADC, and hence to reduce the relative quantisation errors, this new gain is split into an analogue gain (k_{v2}) and digital division (D). Thus;

$$k_v \cdot (k_{v2}/D) = k_i/R_O$$

then $$\underline{k_{v2} = (D.k_i.k_v)/R_O)}$$

Here R_O is the secondary referred value of line surge impedance and it is desirable to maintain k_{v2} in the range $0.5 < k_{v2} < 1$, for reasons mentioned above. The factor D is introduced later in the digital process and for aid of digital division, this is chosen as a multiple of 2.

Prior to analogue to digital conversion, the input phase components of voltage and current are therefore scaled by the following application dependent constants;

voltage gain = cvt ratio x k_v x km x k_{v2} --- 5.12

current gain = ct ratio x k_i x km

5.2.7 ADC

The necessary resolution for converting a +/- 10 V analogue signal into digital form is achieved by a 12 bit (11 bit + sign) ADC. This corresponds to 2^{11} or 2048 levels representing the 10 V input. The conversion gain of the ADC is then simply;

$$kc = 2048/10 = 204.8 \qquad \text{--- 5.13}$$

The range from -10 to +10 V is thus represented by 4096 quantum levels. Because of duty cycle requirements, it is suggested that in hardware form, the ADC should be implemented as a parallel 'bin' type, since these are known to be capable of ultra fast conversion.

5.3 Digital Stages

The first two stages in the digital process involve the use of FIR (Finite Impulse Response) filters which have well defined transient responses and steady state frequency rejection characteristics. The filtering of the signals is carried out digitally since the following advantages are offered as opposed to analogue equivalents;

a) Versatility: The weighting constants governing the response of the filter are simply altered by software re-programming.

b) Accuracy: Background noise introduced by the quantisation of analogue signals can be reduced to well defined, acceptable levels by suitable conversion gain in the ADC stage. Noise in analogue circuits is difficult to quantify since it largely depends upon component tolerances.

c) Freedom from drift: Digital filters exhibit the same characteristics exactly no matter how many times they are used. Analogue filters suffer from component ageing and in many circumstances from changes in temperature.

The digital filtering stages are readily implemented in machine code and as such they are ideally suited to this application.

5.3.1 Superimposed Component Extraction

In order to reject all steady state components, including the power frequency fundamental and all harmonics, a two stage cascaded FIR filter, as shown in Fig 5.4 is utilised. The 'Z' domain transfer function is given by;

$$T1(Z) = (1 + Z^{-n})(1 - Z^{-2n}) \qquad \text{--- 5.14}$$

Where n is the number of discrete samples contained in half a cycle of power frequency. Such an arrangement corresponds to the time domain summation arrangements as shown in Fig 5.6. Substitution of the 'Z' delay operator by exp (jwt), yields the following steady state magnitude/frequency response;

$$|T1(jw)| = 4. \ |\cos(n\theta/2)|. \ |\sin(n\theta)| \qquad \text{--- 5.15}$$

where $\theta = w.\Delta T$

The above function has zero gain at dc. and all harmonics of power frequency, including the fundamental. Such is the response around the latter, that the cascade zero combination lends itself to a less steep cut-off, which then offers high rejection when the input

frequency is subjectto small changes or drift. In this instance, a typical drift of +/- 0.5% does not produce significant spill output from the extraction stages.

The true superimposed component is available at the output of the cascaded extractor for half a period of the power frequency, beyond this time, the measurands contain additional information. This is explained by the fact that the transient data samples, after the half cycle delay, replace those corresponding to the steady state prefault quantities in the filter memory locations.

Although the gain of the extraction filter is in general frequency dependent, the superimposed components appear instantaneously at the output following their arrival and as such, the gain is taken as unity.

5.3.2 Bandpass Filter

Because the fundamental frequency superimposed components contain all of the relevant information appertaining to a particular fault condition, an ideal relaying scheme would involve the use of the these components alone. However, the filtering of all additional high and low frequency components, accompanying the power frequency variation, would introduce significant delay into the measuring process. Indeed, this is a central limitation to the operating speed of distance protection. The new relay, based on fundamentally new principles, is capable of rendering a secure decision from the total superimposed quantities, but the persistance of travelling waves or subsynchronous components within the primary system is

reflected in the measurands for some considerable time after fault inception. Hence, these additional components not only directly contribute to the high speed decision capability of the relay in the initial post fault period, but also in a derogatory sense to the recovery of full sensitivity. This is explained by the fact that the signals S_1 and S_2 are assumed to be zero before the occurrence of a fault or indeed any other type of disturbance.

It is therefore essential to emphasise the initial signal behaviour at the power frequency and to attenuate the unwanted high frequency components after the relay has rendered a decision.

5.3.2.1 Low Pass Filter

High frequency components, including travelling waves, are attenuated by a low pass type filter, which is realised in digital form with the following function;

$$H(Z) = 1/N\ (1 + Z^{-1} + Z^{-2} + Z^{-3} + \ldots + Z^{-m}) \qquad \text{--- 5.16}$$

This simple geometric progression may be re-written as follows;

$$T2(Z) = 1/N\ (1 - Z^{-(m+1)})/(1 - Z^{-1}) \qquad \text{--- 5.17}$$

Hence the filter performs an averaging type function and on a continuous signal basis, a moving average over a window of 'm' samples, is taken. The rate of rise of any continuous input signal is in this way reduced and the filter therefore exhibits a low pass type characteristic.

Considering the equivalent steady state magnitude/frequency response of the function;

$$T2(jw) = \sin(m+1)\theta / \sin\theta \qquad \text{--- 5.18}$$

where $\theta = w.\Delta T/2$

At dc, and low frequencies, this filter has a very large gain, k and the general form of the above frequency function may be seen in Fig 5.6a. As 'm' is increased, the first frequency zero, f_z, is shifted towards dc, which therefore in steady state terms, rejects correspondingly lower frequency components. However, the number of delay terms in Eq 5.17 is also increased which constitutes a greater propagation delay through the filter. In other words, the lower frequencies are emphasised and if 'm' is very large, the higher frequencies are all but filtered out.

This type of filter then directly increases the delay between the arrival of the superimposed components at the relay location and any subsequent decision taken by the relay. This is because the rate of rise of the filtered signal, and hence the corresponding magnitude difference function, is rather sluggish when compared with the raw signal behaviour. This feature however, is beneficial since any travelling wave corruption of the signals, causing a reversal of directional indication is nullified, because over a longer time period, relative to the transit times associated with long series compensated lines, the signals become dominated by the power frequency and dc offset components.

For the purpose of reducing the post fault residual output of the filter, the low pass stage is designed to attenuate any persistant travelling wave component in the signals, some time after the overall impulse duration of the filter. For any given system, the lowest dominant travelling wave frequency f_{TW}, is given by;

$$f_{TW} = 1/4.Tr \qquad \text{--- 5.19}$$

Where Tr is the transit time from the relaying point to the remote point of reflection. For example the Aerial mode propagation velocity is approximately 300 km/ms, so for a section length of 500 km, the corresponding transit time is simply 1.66 ms hence;

$$f_{TW} = 1/(4 \times 1.66 \times 10^{-3}) = 150 \text{ Hz} \qquad \text{--- 5.20}$$

After the impulse duration of the extraction stages, it is therefore expected that for such a system, the relaying signals would be dominated by 150 Hz components, following a fault near to the peak of the prefault voltage.

For the frequency transfer function of Eq 5.18, it may be shown that the lowest frequency zero is positioned at;

$$f_Z = 1/(m+1).\Delta T \qquad \text{--- 5.21}$$

Where ΔT is the sampling time step.

To ensure that the components around f_{TW} are attenuated, it is necessary to position the first zero below f_{TW} by an appropriate choice of 'm'. Eq 5.21 may then be re-written for 'm' to give;

$$m = [1/(f_{TW}.\Delta T)] - 1 \qquad \text{--- 5.22}$$

Thus for a sampling frequency of 4 kHz, ΔT = 0.25 ms, and for f_{TW} = 150 Hz, 'm' is therefore;

$$m = [1/(150.0 \times 0.25.10^{-3})] - 1$$

or $\underline{m \simeq 26}$

Furthermore, as with the cascaded extraction stages, a combined two stage filter offers a greater definition between the pass and stop bands below and above f_{TW}. The corresponding frequency response of the cascaded version is then given by;

$$|T2(w)| = [\sin(m+1)\theta/\sin(\theta)]^2 \qquad \text{--- 5.23}$$

Fig 5.6b shows a gain/frequency response of such a cascaded filter.

The well known repetitive gain/frequency response of digital filters, which undergoes lateral reflection about the Nyquist frequency, is compensated by the analogue pre-filter at the relay input. As such, the filter may then be described in terms of pass and stop bands, which may only be strictly applied to analogue filters.

As the transit time Tr of Eq 5.19 increases with line length, f_{TW} decreases and a correspondingly greater number of elements 'm', are required to completely filter out the travelling waves. This may, for very low frequencies, introduce considerable delay into the measuring process. In the end, the choice of 'm' is therefore a compromise between the speed of operation and recovery capability. That is to say that a small value of 'm' would enable the relay to render a quick decision, often compatable with UHS requirements, although the recovery time of relay would be extended. The choice

of 'm' is application dependent and is discussed in a later chapter. It is also shown that some degree of averaging leads to a more secure decision process at the limit of sensitivity.

5.3.2.2 Low Frequency Rejection Filter

Associated with faults close to a voltage zerocrossing is the familiar exponential offset in the current waveform. This is analogous to modulating the sinusoidal variation with a d.c. or very low frequency component, which is also very dominant in the secondary phase voltages of cvts, due to relaxation transients, as shown in Fig 5.3. Dependent upon the rate of exponential decay, chiefly governed by the X/R ratios of the source and line, the offset is directly reflected in the relaying signals which then remain finite for many cycles after fault. The cascaded extraction stage does have a zero at dc, but the characteristic is very steep and as such, the very low frequencies undergo little attenuation. It is therefore necessary, to introduce some additional low frequency filtering to improve the recovery time. This is achieved by a digital differencer, not to be confused with a differentiator, which is nothing more than a full cycle extraction stage, with the number of delay elements adjusted accordingly. Hence in the Z plane, the filter is described by;

$$T3(Z) = 1 - Z^{-P} \qquad \text{--- 5.22}$$

with the equivalent frequency transfer function;

$$T3(jw) = j2.\sin(pw\Delta T/2) \qquad \text{--- 5.23}$$

By careful selection of 'p', this sinusoidal function, when combined with the low pass moving average stages, forms a bandpass characteristic. A small value of 'p' gives a very flat response at dc, but this also encroaches upon the power frequency region. If 'p' is too large, then the filter does not influence the superimposed components until after a considerable delay and as such, the low frequency components are, in the main, unattenuated.

A well known characteristic of series compensated systems is the phenomena of subsynchronous resonance (ssr). Under many fault conditions, particularly where the series capacitors stay in circuit for the fault duration, these ssr components may persist in the primary system currents for a considerable post-fault period. As suggested by Ballance and Goldberg [26], the frequency of these components may be estimated by the system inductance and capacitance values, prevalent at the fault instant. Thus unlike travelling waves whose frequency is governed only by transit times, ssr frequencies are dependent upon a wide range of variables such as fault type, distance to fault, source capacities and sequence ratios etc. Hence, a wide subsynchronous frequency range between typically 10 to 42 Hz for a 50 Hz system may be obtained. Thus the filtering of such components, using the foregoing 1f rejection stages is not possible, since they are often very close to the fundamental. Even an equivalent analogue high pass stage is not feasible since the transition from 40 Hz in a stop band to 50 Hz in a pass band would require a very high order filter, with intolerable delay to the measurands in the initial period. It is proposed therefore that the relay should be de-sensitised during a period where the measurands are dominated by ssr in order that the latter are prevented from causing any relay mal-operation. It should however, be pointed out

that the primary simulation programs developed for testing the new relay do not incorporate any countermeasures to ssr, although in practice, the latter appear in many guises [27]. Hence the studies presented herein assume absolute worst case conditions whereas in practice, the recovery period may be drastically reduced due to primary system damping of the ssr components.

Extensive studies have revealed that adjustment of the product $p\Delta T$ to be equal to a quarter of the power frequency period, allows undistorted transmission of the superimposed components through the filter, whilst offering adequte low frequency rejection following the initial post fault period. Moreover, a cascaded version of this differencer improves further the lf rejection and results in the overall gain function;

$$|T3(w)| = 4.\sin^2(pw\Delta T/2) \qquad \text{--- 5.24}$$

Unlike the moving averager, this stage does not affect in anyway, the measurands until after the delay period $p_\Delta T$. Consequently, any delay in the decision process of the relay can be attributed to the low pass stages of the digital filter.

As explained in Chapter 6, it is necessary to evaluate the steady state gain of the digital filter, particularly at the power frequency, for the purpose of estimating minimum signal levels required to operate the relay. Hence, considering the overall gain of the filter;

$$k_f = |T2(w)|.|T3(w)|$$

or $$\underline{k_f = [\sin(m+1)\theta/\sin(\theta)]^2.4.\sin^2(p\theta)} \qquad \text{--- 5.25}$$

For m = 26, p = 20 and ΔT = 0.25 ms, then;

θ = 314.2 x 0.25.10^{-3}/2 = 0.0393

and $k_f = [\sin(1.06)/\sin(0.0393)]^2.4.\sin^2(0.7855)$

ie $\underline{k_f = 986}$

With a maximum signal of 2048 ql, the filtered component magnitude would then be;

986 x 2048 = 2019288 ql

Now with 16 bit arithmetic, the maximum number of quantisation levels is 32000 (approx 2^{15}, with 1 sign bit), hence k_f must be reduced, by a factor of 2, so that the mixiмum signal is less than or equal to 32000. In this case, a division of 64 gives k_f = 15.43 and a maximum filtered power frequency component of 15.43 x 2048 = 31600.

A block diagram of the complete digital extraction and filter stages is given in Fig 5.7, and for the given settings as calculated above, the steady state gain/frequency responses of each stage are illustrated in Fig 5.8. The zero gain points of the extraction stages at all harmonics of the power frequency (50 Hz) are evident in Fig 5.8a, whilst the smooth cut-off or notch characteristic around the fundamental is emphasised in the detailed waveform of Fig 5.8b. The low pass averaging stage response for a 500 km line length, corresponding to m = 26 is shown in Fig 5.8c where the first zero gain point is observed to be just below 150 Hz as required for travelling wave rejection. Fig 5.8d illustrates the low frequency rejection stage response, in which the high attenuation of the dc and very low frequency components is evident, the characteristic

being obtained for $p\Delta T$ = 5 ms. The overall response of the digital stages is shown firstly in Fig 5.8e, whereby a general low-pass type characteristic is observed, upto around 600 Hz. Beyond this frequency, particularly with the voltage channel, the net response of the hybrid relay as a whole would be somewhat dominated by the cvt response. Finally, the detailed waveform of Fig 5.8f clearly highlights the steady state rejection of the filter to power frequency components and those close to dc.

5.4 Voltage Channel Gains K,D

The R_O adjustment factor discussed in Section 5.2.6 comprised of two gains, the first of which was accounted for in the analogue section (k_{v2}). The digital gain, 1/D, is now applied to the filtered voltages, together with a 'source coverage' factor, K, so called since it boosts the relative proportion of superimposed voltage when the effective terminating reactance is low. In this situation, a remote fault condition does not give rise to a significant voltage change at the source terminals, usually in the vicinity of the relay. It is recalled that it is the relative polarities and not magnitudes of the voltage and current components from which a directional criteria is formed and as such, the gain K does not invalidate the latter.

5.5 The Decision Process

5.5.1 Trip Counter

To enhance the security of any directional decision based upon the established magnitude criteria, the relaying signals are compared

over a number of samples, by introducing a trip counter. The counter is designed to count in a positive sense upto a decisive level if the signal magnitudes indicate a forward fault and negative for a reverse fault. Particularly under small signal conditions, the levels of noise either from the system or the relay hardware may be appreciable when compared to the magnitude of the superimposed voltage and current signals. Hence a pre-requisite of the counting process is that the measurands must exceed a preset minimum threshold level, since noise may degrade the reliability of the decision. Moreover, in accordance with conventional blocking mode schemes, it is essential to ensure that the relay which should indicate a reverse disturbance should always do so regardless of whether the forward looking relay responds or not. This is achieved by applying a different minimum threshold for forward and reverse faults when the signals are dominated by the voltage component. A forward to reverse threshold ratio of 2:1 is often encountered and the reverse threshold level then sets the absolute minimum which should be above all expected noise levels. The value of the minimum threshold level is discussed in the next Chapter.

For the magnitude criteria alone, an up count is permitted if $|S_2| > |S_1|$, which may be written;

$$DM = |S_2| - |S_1| \qquad \text{--- 5.26}$$

So that DM is +ve for a forward fault and -ve for a reverse fault. Successive up counts will ensue if upon the concurrent samples DM remains +ve, and if the voltage and current components remain above the threshold. After attaining a count of 5, the relay indicates a

forward fault, with the latter figure being optimised from a consideration of speed, sampling frequency and security of decision. As explained in Chapter 4, however, faults close to the zerocrossing of the voltage waveform result in correct directional indication for only a very small initial period. The problem is aggravated by the averaging low pass filter which tends to emphasise this fundamental frequency signal behaviour. Moreover, unsymmetrical threshold levels may result in a small up count of say 1, followed by a rapid number of down counts in the subsequent period, increasing the possibility of relay mal-operation. However, the averaging stages produce double integral forms of the measurands, from which, additional signals proportional to the rate of change of the filtered measurands, may be formed. The latter augment the magnitude function DM to enhance the security of decision, with a modified criteria for directional determination taking the form;

DM +ve and DR +ve indicates a forward fault
DM -ve and DR -ve indicates a reverse fault --- 5.27

where $DR = |S_2^1| - |S_1^1|$ --- 5.28

The variation of DR is such that it is always initially of the same polarity as DM, following which there is no period in which both signals are of the opposite polarity simultaneously. Hence, for a forward fault, the following relation is never true;

$DM < 0$ and $DR < 0$

The counting process is therefore stabilised under low level signal conditions, particularly for faults close to the voltage zerocrossing, where several up/down counts would occur for a scheme

based upon DM alone. A slightly derogatory effect of the second function is that where a fault would initiate a continual up count for a forward fault, the polarity reversal of DR alone would then inhibit further counting, since relation 5.27 is no longer true. If the initial up count is lower than the decisive level, then a delay is introduced, during which the count is held, until DM and DR are again both +ve. In order to surmount this slight drawback, a two stage counting strategy is introduced;

a) Counter Level < 3

For this situation, the counter may increase only if BOTH functions DM and DR are positive. If the signal levels are such that a count of 3 is not achieved before the reversal of polarity of DR, then the count is held until such time as the agreement is again reached.

b) Counter Level ≥ 3

Having obtained a count of 3, the counting is allowed to continue under the control of either difference function. This tends to overcome additional delays introduced by the second difference check on DR and serves to secure and increase the speed of decision for faults close to the voltage zerocrossing.

The above description is explained for forward faults, but similar -ve counting considerations are applied for reverse faults.

5.5.2 Dynamic Threshold Function

In the discussion of the counting philosophy, it was stated that the superimposed voltage and current components should exceed a minimum threshold level, before the counter is enabled, a feature which provides some degree of immunity in the presence of noise. After rendering a decision however, the relay should be de-sensitised for at least the impulse duration of the filters, since their outputs are then no longer representative of the true superimposed components. More importantly, and specifically related to series compensated lines, is the presence of subsynchronous components which may persist in the primary system for many cycles after fault inception, particularly when capacitor gap flashover does not occur. As mentioned previously, it is virtually impossible to filter such components, since their frequency is dependent upon several factors. Thus the post fault relaying signals may be dominated by the subsynchronous components for a rather long post-fault period and as a direct consequence, may cause relay maloperation if they are above the threshold level.

To overcome the abovementioned problems, a dynamic threshold function D(n) is introduced, which is based upon a moving average of the relaying signals, over a number of samples, such that;

$$D(n) = 1/N \sum_{k=n_1}^{k=n_2} |S_1(n-k)| + |S_2(n-k)| \qquad \text{--- 5.29}$$

When steady state conditions prevail, the signals are nominally zero valued, hence D(n) is also zero. A constant minimum level Dc is therefore introduced for reasons described earlier, which then gives a threshold function of the form;

$$T(n) = Dc + D(n) \qquad \text{--- 5.30}$$

By suitable choice of n_1, a delay between the detection of the superimposed components and a corresponding increase of D(n) is obtained. This directly increases the operating speed of the relay since the latter is most sensitive when only the minimum threshold is applied. After the initial delay, T(n) becomes solely a function of the signal behaviour and once the superimposed quantities die out (steady state conditions regained), the signals fall to zero, with T(n) falling to the minimum level Dc shortly after. The variable n_2 sets the window width over which the moving average is taken and given that the subsynchronous components dominate the post-fault signals, n_2 should be chosen to give a smooth average around the subsynchronous frequency. However, a consideration of the overall steady state frequency response of the total extraction and filtering stages, has led to the conclusion that the window width should correspond to half the fundamental power frequency, since very low frequency components are attenuated the low frequency rejection stage, and frequencies close to the fundamental are attenuated by the cascaded extraction stages. Thus for a 50 Hz system, a window width of 20 ms is selected, since this corresponds to half a period of 25 Hz waveform.

Such a dynamic function stabilises the relay when the latter is subject to subsynchronous components or indeed any spurious inputs, since full sensitivity is regained only when the latter have died out. This enables the relay to recover from an initial disturbance with the minimum of delay, with no possibility of any mal-operations.

A diagram to aid the understanding of the decision process and counter action is illustrated in Fig 5.9, and although not shown, a reset facility is introduced to ensure that the counter is not biased in the wrong sense, when superimposed measurands are generated for proceeding faults. The dynamic threshold is denoted by T, with 2T being the required level for the detection of disturbances in the forward direction to the relay.

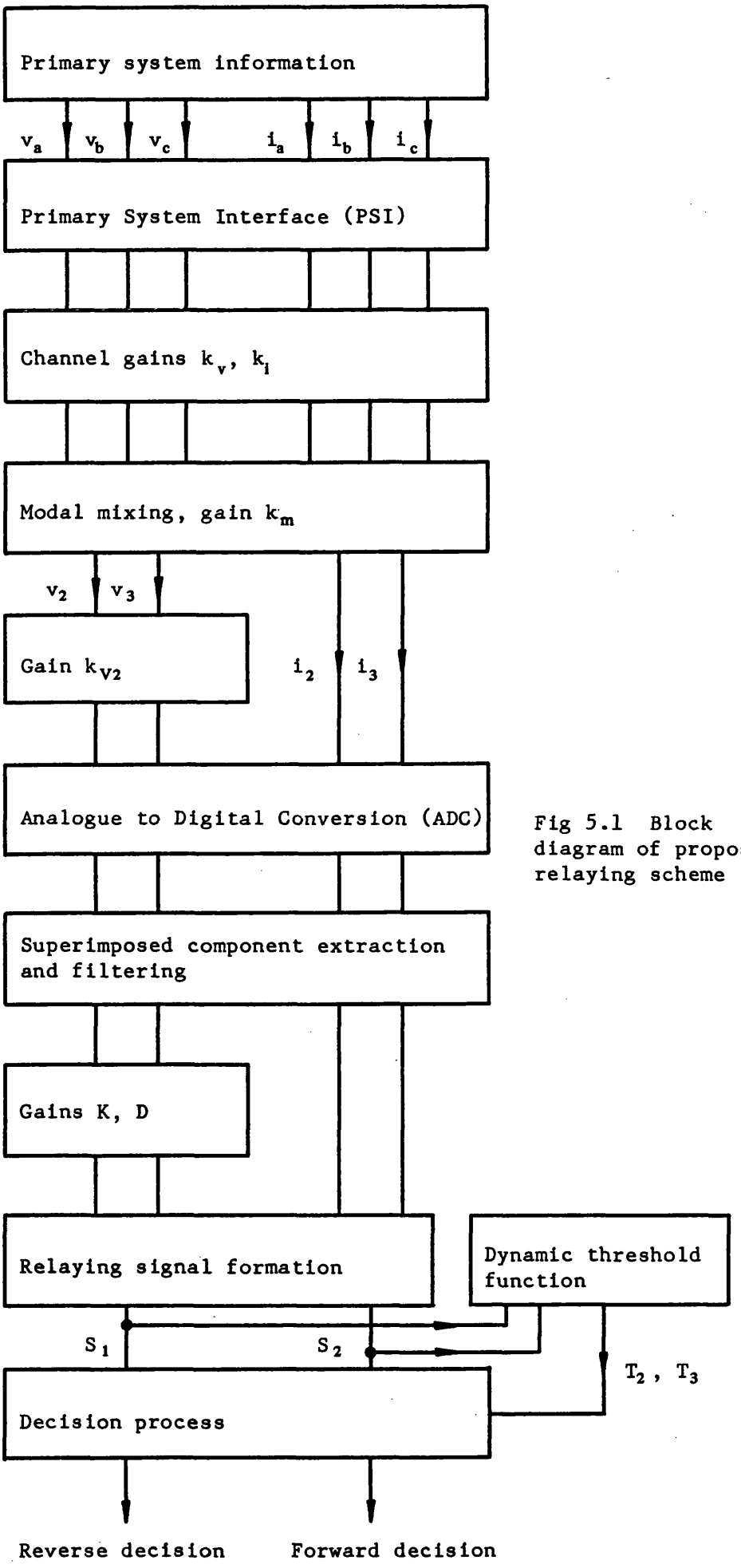


Fig 5.1 Block diagram of proposed relaying scheme

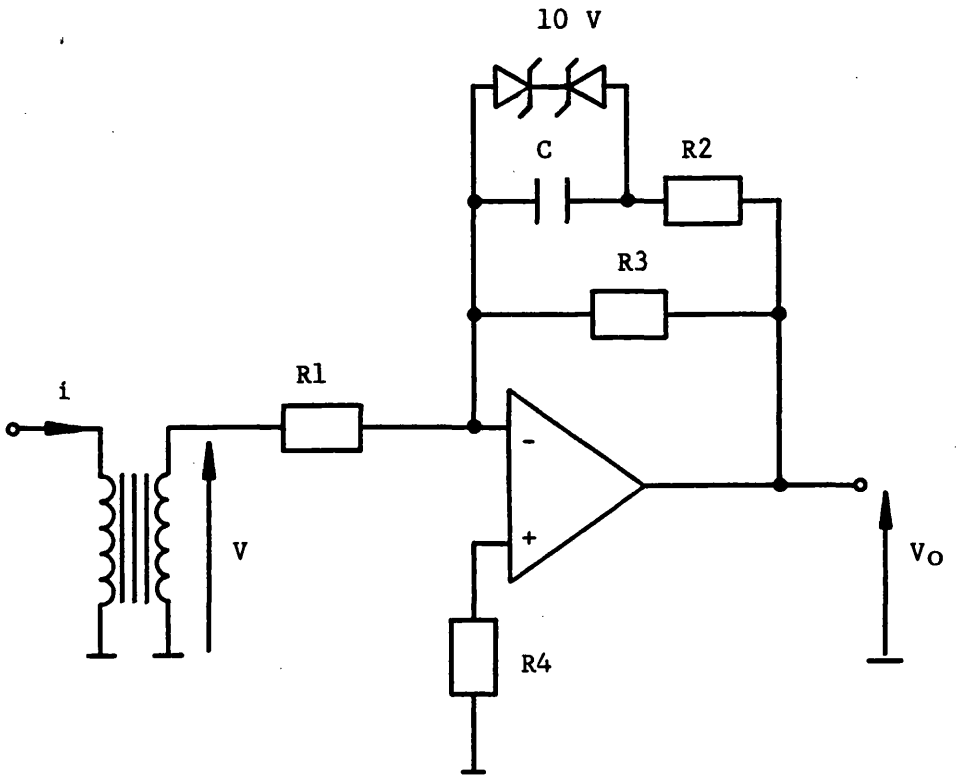
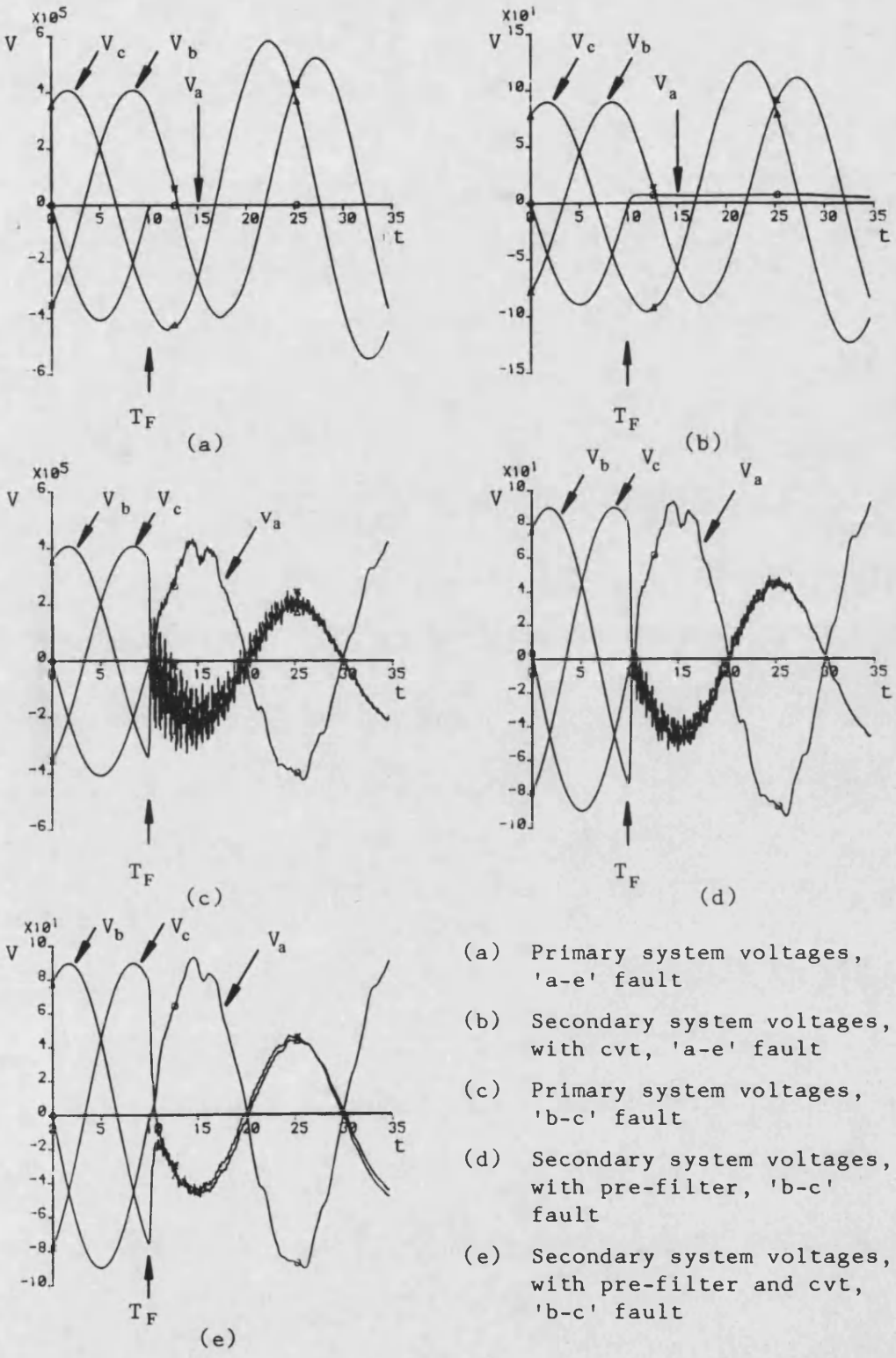


Fig 5.2 Current input module (CIM)



(a) Primary system voltages, 'a-e' fault

(b) Secondary system voltages, with cvt, 'a-e' fault

(c) Primary system voltages, 'b-c' fault

(d) Secondary system voltages, with pre-filter, 'b-c' fault

(e) Secondary system voltages, with pre-filter and cvt, 'b-c' fault

Fig 5.3 Waveforms highlighting cvt and pre-filter responses for 'a' phase to earth fault, 0^{o} fia and 'b' to 'c' interphase fault, 90^{o} fia

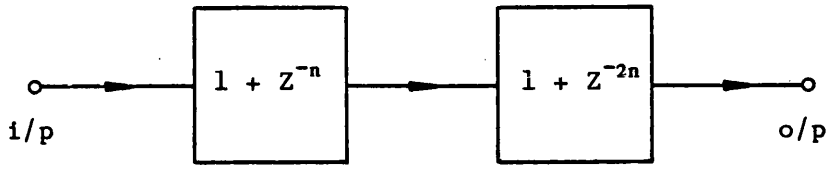


Fig 5.4 'Z' plane block diagram of superimposed component extraction circuit

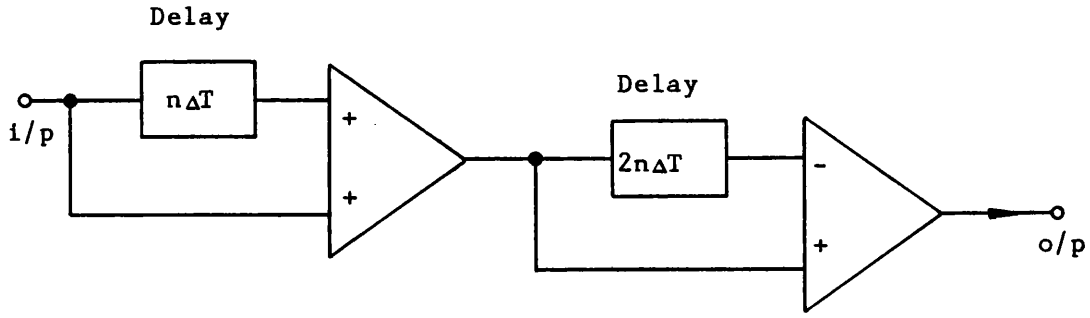
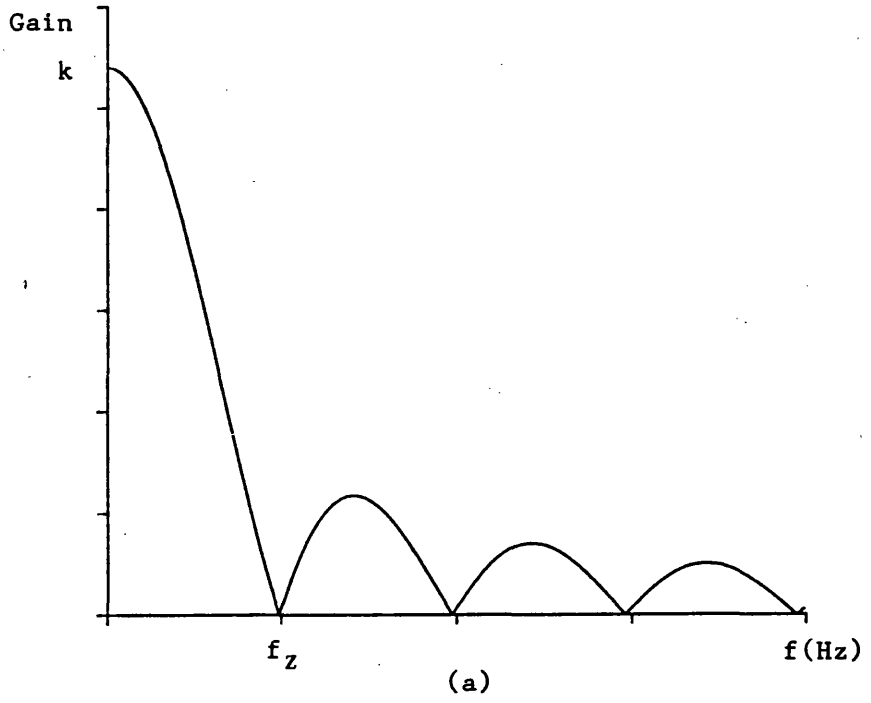


Fig 5.5 Operational amplifier equivalent of superimposed component extraction circuit



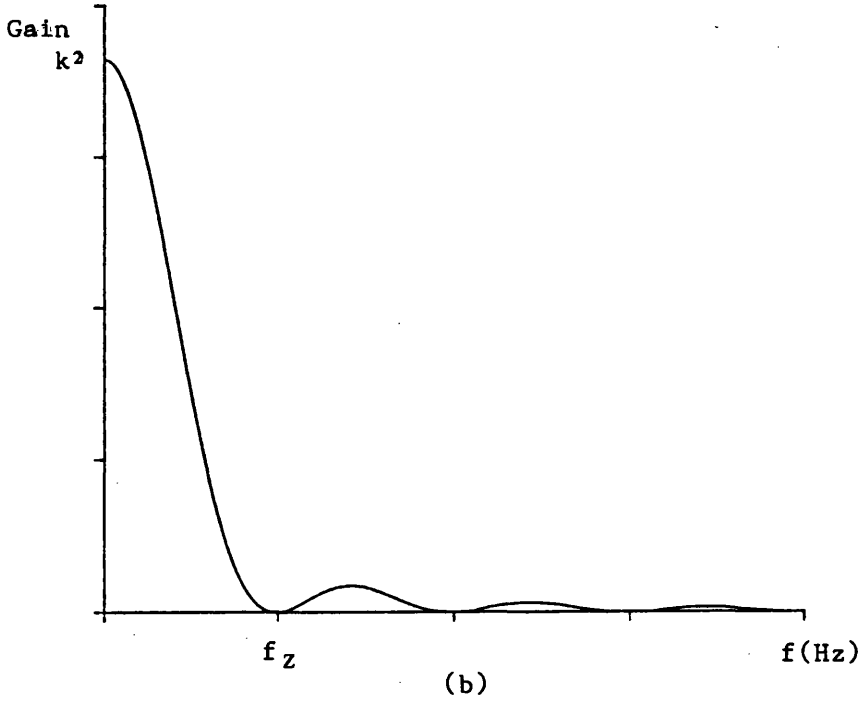


Fig 5.6 Averaging filter frequency response

(a) Single stage
(b) Cascaded stages

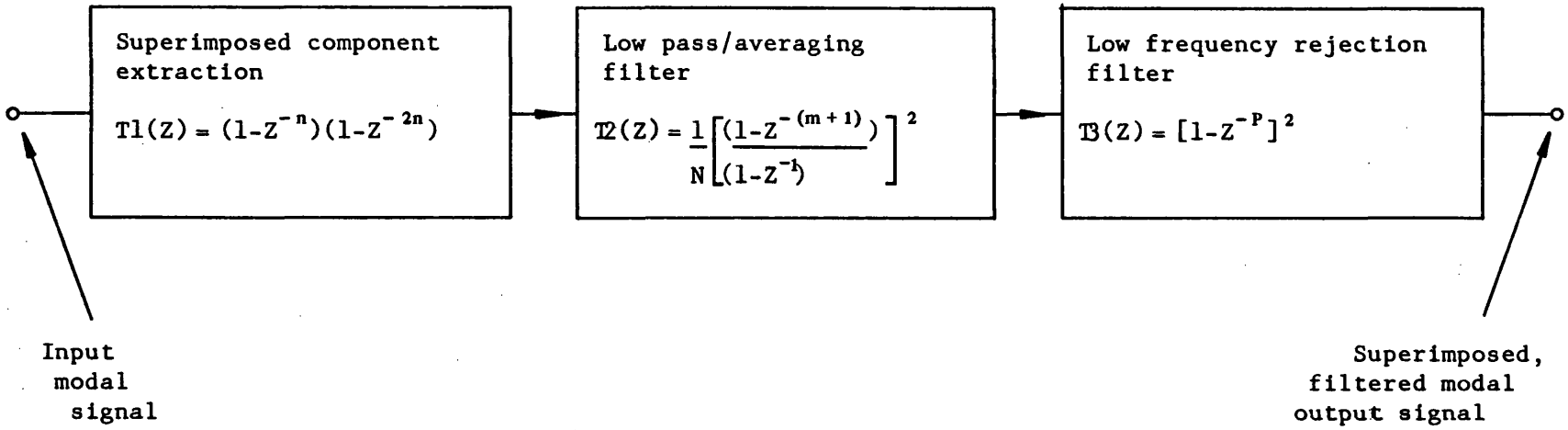


Fig 5.7 Block diagram of digital extraction and filtering stages

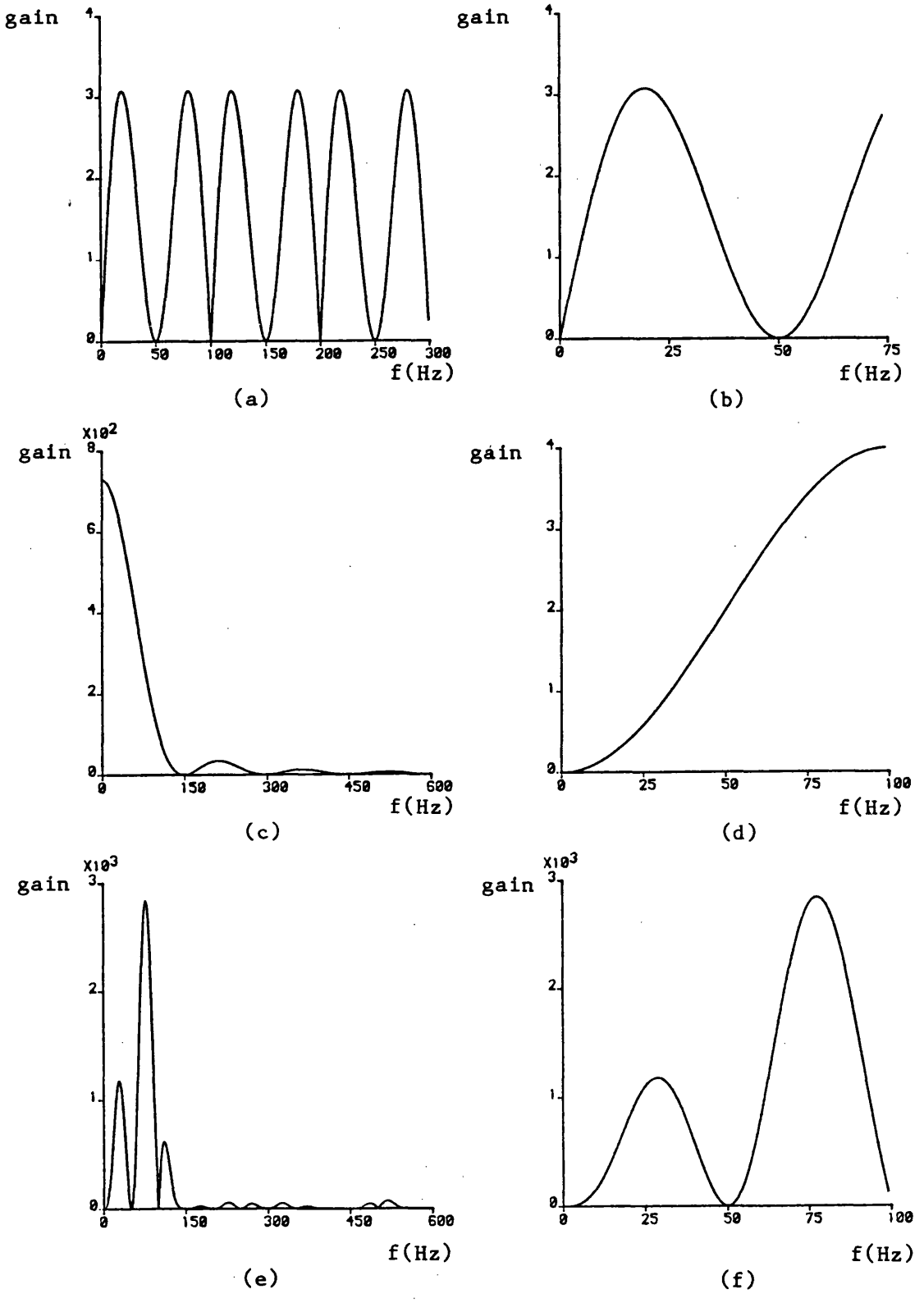
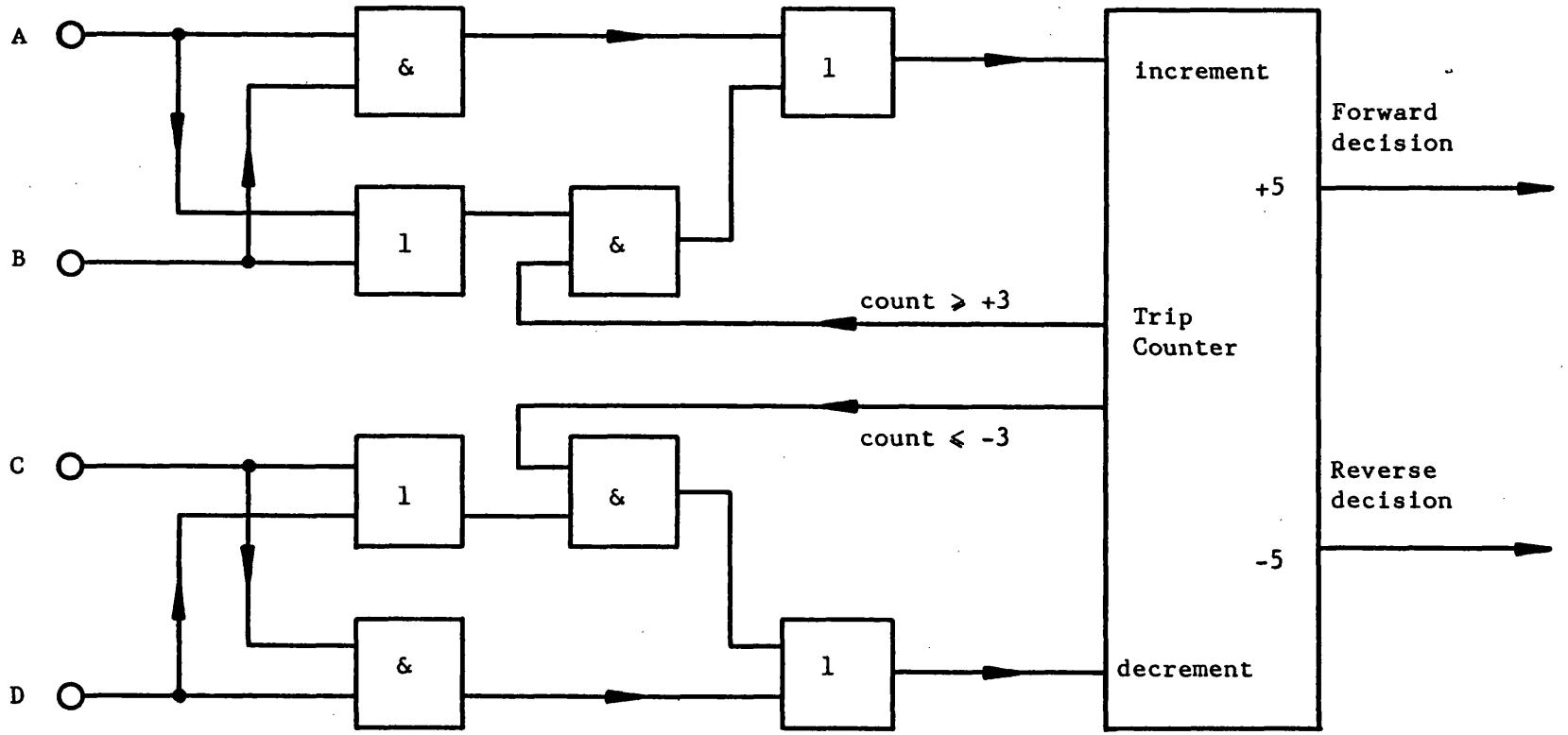


Fig 5.8 Frequency responses of digital stages

(a) and (b) Extraction stages
(c) Averaging filter
(d) Lf rejection filter
(e) and (f) Overall digital filter



A = 1 when |DM| > 2T and DM +ve
B = 1 when |DR| > 2T and DR +ve
C = 1 when |DM| > T and DM -ve
D = 1 when |DR| > T and DR -ve

Fig 5.9 Decision process/trip counter logic diagram

CHAPTER 6: APPLICATION SETTING PROCEDURE

For any given system application, the relay constants described in Chapter 5, must be adjusted for optimum performance. The methods by which each constant is set are best explained with reference to an actual system model, following the recommended setting procedure outlined later in this Chapter.

6.1 Current Interface Constant k_i

Firstly, the gain k_i which basically influences the sensitivity of the relay must be set in accordance with the mode of protection employed. As mentioned in Chapter 5, the proposed scheme is configured in a blocking mode, ie the relay initiates local breaker tripping if, after a co-ordination delay, no block signal is received from the remote end. The major disadvantage of directional comparison schemes is that their reach is not well defined in say secondary impedance terms and as such, many block or restrain actions may be taken, for remote disturbances, by the unit scheme as a whole. It is then imperative that the relays regain full sensitivity with the minimum of delay such that internal faults, occurring shortly after the remote disturbance, are quickly detected. Such action is not possible when the current channel is permitted to clip and therefore the gain k_i must be calculated on the basis that the maximum external or through fault current does not cause clipping in the analogue stages. The largest currents are expected under three phase fault conditions located in the position F1, indicated in Fig 6.1. The system calculations are executed assuming the system is single end fed, since a high capacity source behind the relay at P

would cause the largest fault current, I_F, to flow in such a situation. Moreover, since current waveforms are in general dominated chiefly by low frequency components as opposed to relatively noisy voltage waveforms, symmetrical component calculations yield very good approximations to the actual currents that would flow. In this instance, the source and line pps parameters (ignoring resistance) only are required due to the nature of the fault type. The simple pps equivalent circuit drawn for the fault location F1 of Fig 6.1 is then given in Fig 6.2, from which;

$$I_F = E/(Z_L + Z_S) = E/X \qquad \text{--- 6.1}$$

where E = phase rms voltage

Z_L = pps line impedance

Z_S = pps source impedance (in this case at end P)

The Laplace analysis of a suddenly applied forcing voltage to an inductive circuit generates a current scaling factor of;

$$1 - \cos(wt) \qquad \text{--- 6.2}$$

Thus for wt = 180 degrees, ie half a cycle, the current is twice the E/X value, ie, it is fully offset. For series compensated lines, if the capacitors remained in circuit until steady state fault conditions are reached, Eq 6.1 becomes;

$$I_F = E/(Z_L + Z_S - Z_C) = E/XX \qquad \text{--- 6.3}$$

where Z_C = power frequency capacitive reactance

In this case, the current scaling factor is given by;

$$\cos(wt) - \cos(at) \qquad \text{--- 6.4}$$

Where a is derived from the total circuit inductance, L and capacitance, C such that $a = 1/LC$. Such an expression also has a maximum of 2, but the build up of current in this case is unlike the plain feeder behaviour. As the degree of series compensation increases, the offset is progressively delayed, but the subsequent operation of the capacitor protective gaps serves to limit the large currents which build up, since the effective line impedance is increased after gap flashover. Dual gap schemes with non-linear resistors tend to reduce the degree of compensation rather than suppress the latter during by-pass conditions, but nevertheless, the subsynchronous component is severely damped thereby minimising any offset of the line current. It should be noted that for systems which permit the total switching out of series compensation, the current scaling factor is then the same as for the plain feeder case and calculations must then account for a fully offset condition.

The voltage developed across the series capacitors is a time integral of the current flowing in them, hence there is a small delay between the build up of large currents and the operation of the spark gaps. Extensive studies have revealed that for a practical range of series compensation of 30 to 70% and an extreme gap setting of 4 pu, the maximum external fault current, for a source capacity of 35 GVA, does not exceed 1.15 times the calculated value, whether the compensation is located centrally or at the line ends. Thus for a fault current level based upon Eq 6.3, a scaling factor k is introduced, which including a small error margin of 10%, is taken as 1.25.

The secondary referred value of the product $k_O.I_F$ is taken for the evaluation of the current interface constant k_i, and in accordance with standards for conventional protection, a load current I_L of 4 amps secondary is added to that figure. Thus recalling Eq 5.8;

$$k_i = 10/1.414(k_O.I_F + I_L) \qquad \text{--- 6.5}$$

6.2 Voltage Gains k_{v2} and D

The primary system aerial mode surge impedance is, for an ideally transposed system, equal to 300 Ω. Simulation of a practical system has however, revealed a more realistic figure of R_O = 286 Ω (horizontal construction). The secondary referred value of R_O is then given by;

$$R_O(\text{sec}) = R_O(\text{pri}) \times \text{vt ratio} \times \text{ct ratio} \qquad \text{--- 6.6}$$

Once k_i is determined as above, k_{v2} and D may then be found by substitution of the secondary referred value of R_O into Eq 5.11 as follows;

$$k_{v2}/D = k_i/k_v.R_O$$

6.3 Voltage Channel Gain K and Noise Considerations

The source coverage factor K is included to boost the level of superimposed voltage when the relay is in close proximity to a low impedance source. In such situations, a remote fault would generate little change in the relaying point voltage and is compensated by increasing K, which does not invalidate the directional criteria established previously. However, accompanying the increase in voltage signal level is an associated increase in the noise levels in

the voltage channel. The make up of power system noise which is also associated with the current channel, may be thought of in four categories;

a) Low level noise generated by remote disturbances, ie switching, tap changing etc.

b) Background noise from the analogue hardware section of the relay.

c) Spurious components at the outputs of the extraction stages as the system frequency drifts.

d) Quantisation noise introduced by analogue to digital conversion.

Noise from source (c) is effectively removed by employing the dual extraction stages (full and half cycle extractors) and by suitable choice of a large quantum level range (+/- 2048), quantisation errors are virtually eliminated.

It is recalled from the previous Chapter that the decision process is only actuated once both the voltage and current signals exceed the minimum threshold levels. Such levels are therefore based upon system and hardware noise mentioned above. Peck [25], from his unique field trial monitoring tests on part of the UK supergrid system, has confirmed that the bulk of the day to day noise conforms to a Gaussian type characteristic, but specific levels are in fact difficult to quantify. It is expected that for large interconnected systems such as in the UK, the overall levels of noise would be substantially greater than the more independent or 'weak' series compensated networks. Moreover, the noise levels at either end of a

protected zone whch has a great number of feed round paths as expected to be more or less equal, whereas with very long line applications, there may be negligible local noise relative to that generated at the remote load centres. As such, the levels of background noise for the latter are difficult to predict and further in situ monitoring tests on an actual series compensated system are required at a later date.

Some degree of engineering judgement must therefore be applied to estimate a realistic minimum threshold level for the CAD studies considered here. Considering the current channel, as the length of protected line section increases the gain k_i is also increased, thereby increasing the relative current signal noise levels. Thus it is forseen that the threshold level will take the form of Eq 6.9;

$$T_{MIN} = C + D.I_F \text{ or } C + D^1/k_i \qquad \text{--- 6.9}$$

$$(\text{since } I_F \propto 1/K_i)$$

Where C is a constant derived from relay hardware noise estimates and I_F is the maximum external fault current which if exceeded would result in current channel clipping. Barker [21], in his work on directional protection of plain feeders, has developed relationships between line length, I_F and T_{MIN} for the maximum encountered source capacity (minimum source impedance), such that T_{MIN} varies from 19 to 23 quantum levels for line lengths of 0 to 250 km respectively. Subsequently, a relationship is developed between the source coverage gain K and the line length, in order to equalise the noise levels in both channels.

Such estimates are based entirely upon theoretical figures which have been shown to be quite pessimistic from results using prototype equipment in the working environment. Peck [25] suggests that a minimum level of 14 is sufficient for the system considered, if occasional counting of +/- 1 is permitted, the latter figure being well below the decisive level of 5. Moreover, a detailed analysis of the characteristics of the superimposed voltage and current components, has highlighted the necessity for applying different thresholds to each channel in order to improve the overall sensitivity and hence coverage of the scheme. It must be emphasised that the above results are obtained on a specific system and with relaying parameters set from CAD studies. However, they give some indications that the aforementioned range of T_{MIN} between 19 and 23 ql is quite acceptable for use in the design stage. For the series compensated systems under consideration a minimum threshold of 20 ql is therefore considered to be realistic enough in order that the capability of the scheme be assessed. There is also enough evidence to suggest that this setting is perhaps slightly pesimistic and as such may in fact be lowered when more information is obtained from series compensated system field trials.

In setting the relay constants, k_i and K must therefore be selected as those minimum values, which limit the degree of noise into the decision process, whilst ensuring adequate fault coverage. It is then possible to derive a relation between the nominal rms modal input signal and the process gains, which would result in a processed digital signal level equal to the minimum threshold, as follows;

$$Ismnom \times [1.414.k_i.k_m.k_c.k_f] = Ith$$

and $$Vsmnom \times [1.414.k_v.k_{v2}.k_m.k_f.K/D] = Vth \qquad \text{--- 6.10}$$

Eq 6.10 enables estimates of the nominal input quantities to be made, but such values do not ensure relay operation. This is due to the fault point on wave effect, whereby the initial signal energy content, with respect to the threshold levels selected, may be insufficient to guarantee fault detection. For this reason, an investigation into the point on wave sensitivity for the most extreme system parameters likely to be encountered in practice, was carried out, using a realistic system simulation. For a range in source capacity of 0.5 upto 20 GVA, 70% series compensation and 500 km line length, it has been found that the minimum input levels required to ensure relay operation for each point on wave fault, are related to the nominal values by;

$$Ismmin = 23.4 \times Ismnom$$

and $$Vsmmin = 6.11 \times Vsmnom \qquad \text{--- 6.11}$$

These factors may then be substituted into Eq 6.10 to give;

$$Ismmin = \frac{23.4 \times Ith}{[1.414.k_i.k_m.k_c.k_f]} \qquad \text{--- 6.12}$$

and $$Vsmmin = \frac{6.11 \times Vth}{[1.414.k_v.k_{v2}.k_m.k_f.K/D]} \qquad \text{--- 6.13}$$

Once k_i is set and the filter transfer functions optimised for the given system, Eq 6.12 then yields a minimum level of input current, in terms of Ith, required to operate the relay. For the same system, the minimum input voltage is related to Vth and K, so that a knowledge of the minimum superimposed voltage presented to the relay will enable a value of K to be found to ensure operation when the decision process acts upon the voltage signal alone. As mentioned above, an upper limit is placed upon the gains k_i and K, relative to the thresholds employed, but without accurate system data, the setting procedure below yields only the minimum values required. Values of K higher than those determined would be desirable since the rate of rise of the voltage signals would be increased which in some circumstances, would result in faster relay operation.

Estimates of Ismmin and Vsmmin for a given system are difficult to make due to the distributive nature of transmission lines and the variation in the point on wave instant at which a fault occurs. Certain approximations are therefore necessary and the method of symmetrical components may be applied to establish the order of magnitude of the superimposed quantities. The latter values differ from those obtained from a realistic simulation for the above reasons and particularly with the current component, because the series capacitors tend to reduce the rate of rise of current in what is effectively a second order network. Thus the assumption of values of the pps, nps and zps impedances of the capacitor banks are somewhat unrealistic to the steady state values. More importantly, the transient response of the averaging filter is assumed to be equal to that during steady state conditions, ie the power frequency gain

factor is taken. As with all digital filters however, such an approximation is somewhat unrealistic since a minimum delay period equal to the impulse duration of the filter is necessary before steady state characteristics can be assumed. However, provided the current and voltage scaling factors of 6.11 and 23.4 are applied, symmetrical component diagrams give good indication as to the limits of the relay's coverage.

For the single end fed system of Fig 6.1, a single phase to ground fault on the line side of the remote end capacitor (fault position F2) will generate the smallest magnitude of superimposed components at the relay location near P. The interconnected phase sequence diagram of Fig 6.3 is applicable for this type of fault, and with the following assumptions;

$$Z_{LO} = 3.Z_{L2} \text{ and } Z_{SO} = Z_{S1} = Z_{S2},$$

the total line impedance Z_L is given by;

$$Z_L = Z_{LO} + Z_{L1} + Z_{L2} = 5.Z_{L1}$$

For the capacitor bank, $Z_{CO} = Z_{C1} = Z_{C2}$, so that the total capacitive reactance is;

$$Z_C = Z_{CO/2} + Z_{C1/2} = 3.Z_{C1/2}$$

Thus the total impedance of the line and capacitor bank Z_T, is given by;

$$Z_T = 5.Z_{L1} + 3.Z_{C1} \qquad \text{--- 6.14}$$

Similarly for the end P source;

$$Z_S = 3.Z_{S1} \qquad \text{--- 6.15}$$

As the interconnection yields a current component equal to $I_{Fa}/3$, the above impedances are divided by 3 to determine the equivalent phase quantities. Thus;

$$Z_T = 5.Z_{L1/3} + Z_{C1/2} \text{ and } Z_S = Z_{S1}$$

If such values are then referred to the secondary system, a general superimposed phase component diagram may be constructed as shown in Fig 6.4. The reference quantity of the voltage axis is the 1 pu nominal seconary voltage and clearly shown are the minimum levels of superimposed voltage and current that would be measured at end P. Assuming then a Karrenbauer modal transform, the estimates in modal terms are then simply the phase quantities divided by 3. To illustrate the procedure for a given system, the following parameters are considered;

Line length = 500 km — Line voltage = 500 kV

Line Zpps = 0.31 Ω/km — 70% series compensation

cvt ratio = 110/500000 — ct ratio = 1200 : 1

Max source capacity 20 GVA, minimum 0.5 GVA

For these parameters;

$Z_{L1} = 500 \times 0.31 = 155\ \Omega$

$Z_{C1} = -(155 \times 0.7) = -108.5\ \Omega$

hence $Z_T = (5.155/3) - (108.5/2) = 204.8\ \Omega$

With the 20 GVA source;

$Z_{S1min} = (500000)^2/20 \times 10^9 = 12.5\ \Omega$

and the 0.5 GVA source;

$$Z_{S1max} = (500000)^2 / 0.5.10^9 = 500\ \Omega$$

Each of the above impedances are referred to the secondary by multiplying by the cvt and ct ratios to give;

$$Z_T = 53.87\ \Omega$$

$$Z_{S1min} = 3.30\ \Omega$$

and $Z_{S1max} = 132.00\ \Omega$

Now the nominal secondary rms phase voltage is simply 110/1.732 = 63.5 volts, hence the diagram of Fig 6.5 may then be constructed. From this diagram, the minimum expected phase quantities are found, but simply graphical relations yield more accurate values as follows;

$$Isamin = 63.5/[Z_S + Z_T]$$

and $Vsamin = Isamin \times Z_S$ --- 6.17

Thus for the 20 GVA source, Eqs 6.17 give;

$$Isamin = 63.5/[3.3 + 53.87] = 1.11\ A$$

and $Vsamin = 1.11 \times 3.3 = 3.66\ V$

which yield corresponding modal component magnitudes of;

$$Ismmin = 1.11/3 = 0.37\ A$$

and $Vsmmin = 3.66/3 = 1.22\ V$ --- 6.18

For the 0.5 GVA source, similar relations yield;

$$I_{smmin} = 0.113 \text{ A} \qquad \text{--- 6.19}$$

and $V_{smmin} = 15$ V

The quantities of Eq 6.18 and 6.19 are then substituted into Eqs 6.12 and 6.13, together with the optimised gain constants to determine if all faults on the system would be successfully detected. At this stage, it is beneficial to go through an entire setting sequence, as detailed below, utilising the same typical system parameters given above.

6.4 Example Setting Procedure

In addition to the aforementioned parameters, the primary surge impedance value is required for determining the appropriate relay settings;

R_O = 282.6 Ω (primary) = 74.6 Ω (secondary)

As described in Chapter 5, a line voltage of 500 kV produces a fixed k_v gain of 0.0557 and with the 20 GVA source, the equivalent pps impedance was calculated above as 12.5 Ω. Now with the total pps line impedance of 155 Ω and 70% compensating reactance of 108 Ω, then the maximum through fault current I_F is determined from Eq 6.2 as being;

$$I_F = (500/1.732)/(155 + 12.5 - 108.5)$$

or I_F = 4.892 kA (4.08 amps secondary)

Thus with an offset correction factor k_O of 1.25;

$$k_i = 10/(1.414[1.25 \times 4.08 + 4])$$

ie $\underline{k_i = 0.777}$

Then $k_{v2}/D = k_i/(k_v \times R_O)$

ie $k_{v2}/D = 0.777/(0.0557 \times 74.6) = 0.187$

Thus, for $0.5 < k_{v2} < 1$, the value of $D = 2^n$ is 4, hence;

$$k_{v2} = 0.187 \times 4$$

or $\underline{k_{v2} = 0.748}$

The gains k_m and k_c are fixed at 1.732 and 204.8 and are independent of the system application. Moreover, if the digital filter is adjusted for rejection of the travelling wave components as described in Chapter 5, then for the 500 km line length considered, the gain k_f is identical to that evaluated previously, this being (after division of 64) equal to 15.43. Thus from Eq 6.12 the required minimum current level is given by;

$$\begin{aligned} Ismmin &= 23.4 \times Ith/[1.414 \times k_i \times k_m \times k_c \times k_f] \\ &= 23.4 \times Ith/[1.414 \times 0.777 \times 1.732 \times 204.8 \times 15.43] \\ &= \underline{3.89.10^{-3} \times Ith} \end{aligned}$$

and $Vsmmin = 6.11 \times Vth/[1.414.kv.kv2.km.kc.kf.K/D]$

$$= \frac{6.11 \times Vth}{[1.414 \times 0.0557 \times 0.589 \times 1.732 \times 204.8 \times 15.43 \times K/4]}$$

or $\underline{Vsmmin = 0.076 \times Vth/K}$

Now with a forward to reverse threshold setting of 2:1 for the current channel, Ith is therefore taken to be 40 ql, whilst Vth is 20 ql. With these values;

Ismmin = 0.156 A and Vsmmin = 1.52/K

Recalling the minimum values of Ismmin and Vsmmin for the system;

Ismmin = 0.37 A and Vsmmin = 1.22 V.

Thus the superimposed modal current generated by the remote fault is sufficient to ensure relay operation, but the voltage signal is too low. By setting K equal to 3, the actual quantities presented to the decision process are then approximately twice those required for operation, in each channel. Such levels provide a substantial allowance for any noise content within the signals, which in any event is not expected to exceed 50% of the minimum threshold.

If now the relay settings based upon the 20 GVA fault level are maintained and the fault level subsequently reduces to 0.5 GVA, the voltage component is significantly larger than the previous case, but the minimum current, from Eq 6.20 is only 0.113 A. It must therefore be concluded that for the typical maximum line length encountered in practice of 500 km, a 70% series compensated, single end fed system cannot be protected by this relay, if the equivalent fault level behind the relay is permitted to change over such an extreme range. Conversely, if the relay constants are set for maximum fault level of 500 MVA (0.5 GVA), then current clipping for internal faults would then be a distinct possibility, which is totally unacceptable with regard to unit protection scheme as a whole. Thus the findings of this investigation reveal that wide ranges in a fault levels cannot be tolerated, but further studies have shown that by reducing the range from 900 MVA to 20 GVA, or from 400 MVA to 1.8 GVA, such a

system can be reliably covered. Moreover, the minimum fault level necessary for relay operation when the decision process is controlled by the superimposed current is for a 500 km line equal to 300 MVA. Below this figure, insufficient current is generated by the fault to ensure fault detection for all pointson wave. The latter figures are in fact more realistic when series compensated systems with long continuous (no outfeeds) line sections are involved.

It must be stressed that the foregoing discussion offers some initial estimates of the relay capability for single end fed systems, although further investigation is necessary for determining the range of fault level coverage between two sources at either end of the line being protected. Moreover, field testing at a later stage may also reveal more accurate noise information which is expected to prove that lower threshold levels than those adopted would still maintain relay security and hence improve the coverage of the latter.

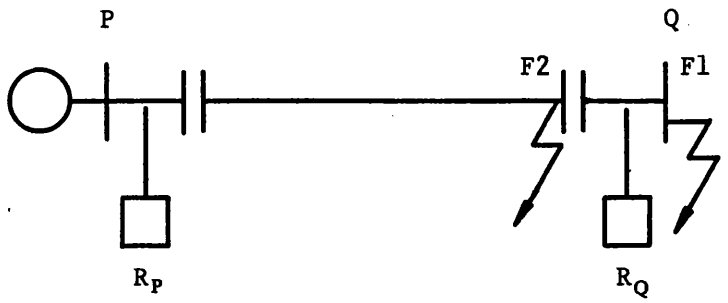


Fig 6.1 Single end fed system showing fault positions F1 and F2 used in relay setting procedure

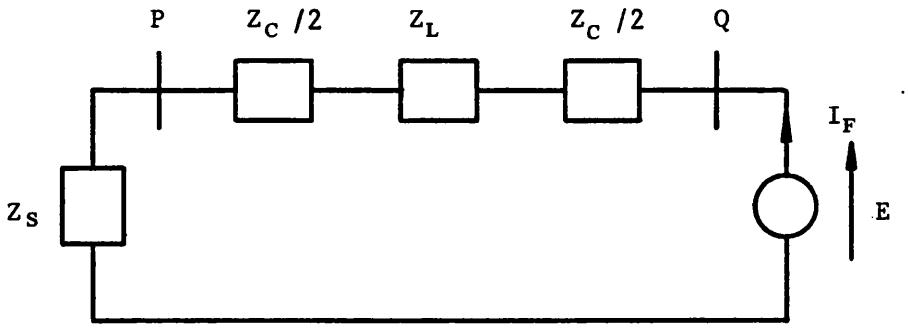


Fig 6.2 PPS equivalent circuit for 3 phase to earth external fault at F1

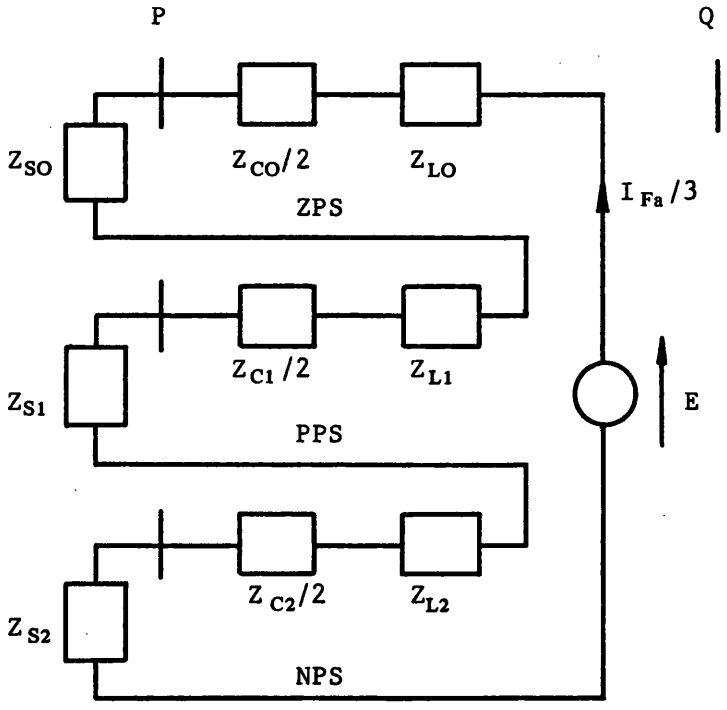


Fig 6.3 Phase sequence equivalent circuit for 'a' phase to earth fault at point F2

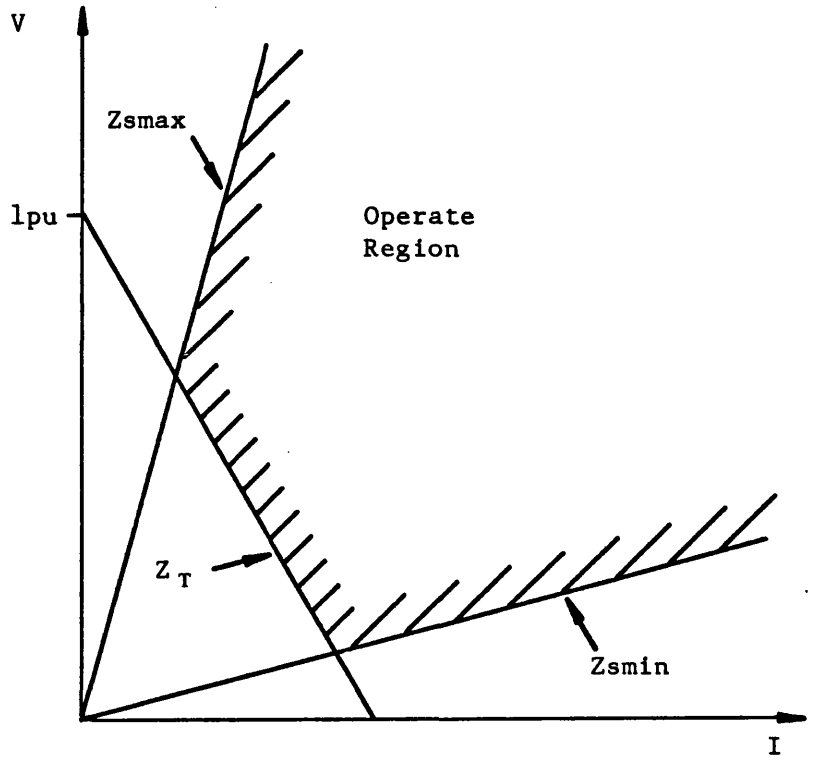


Fig 6.4 General phase superimposed component diagram showing minimum levels required for relay operation

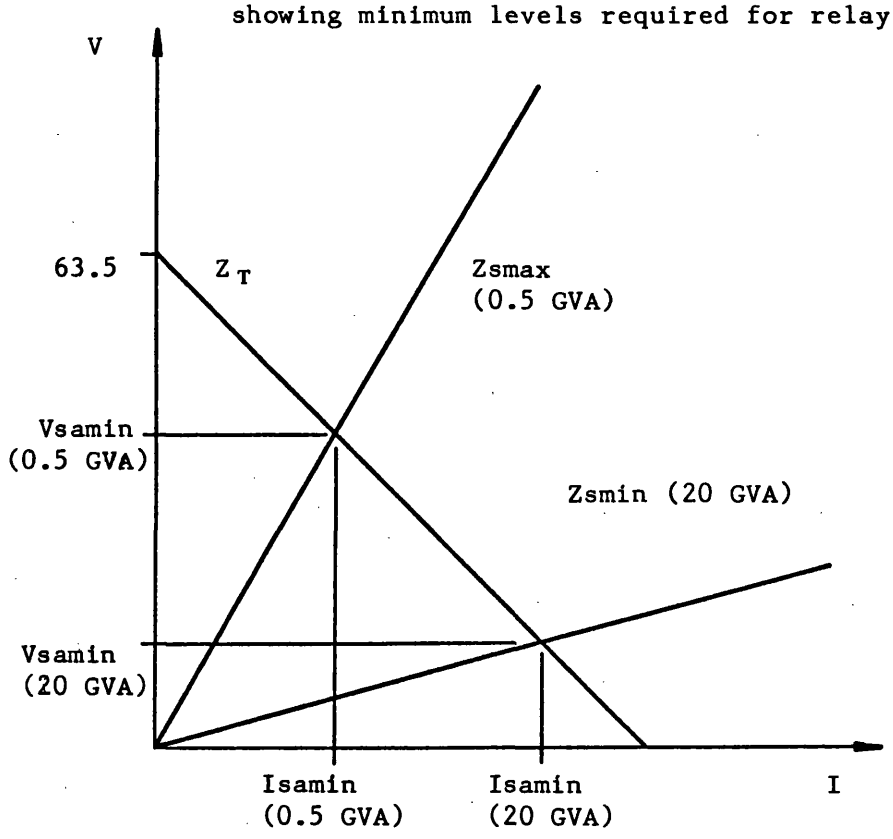


Fig 6.5 Phase superimposed component diagram with source capacities of 0.5 and 20 GVA

CHAPTER 7: RELAY PERFORMANCE EVALUATION

The majority of results presented in this Chapter are obtained from a simulation model of a single circuit series compensated system with compensation either at the midpoint or at the line ends. Also included are some interesting results for double circuit systems. The basic systems studied are shown in Figs 7.1 and 7.2 for single and double circuit applications respectively. The fundamental relay operating principles are illustrated by figures relating to the outputs at the individual relay stages described in Chapter 5, during typical fault conditions. The line construction details of the systems are given in Appendix A7.1, together with the line and earth parameters. In this respect, the commonly encountered horizontal tower arrangements associated with long line applications are used throughout.

7.1 Typical Fault Studies to Explain Operating Principles

7.1.1 Compensation at Line Ends

The first group of tests relate to the single circuit system of Fig 7.1, in which the terminating sources comprise of a general source model based upon abitrarily defined short circuit levels [17]. The extreme source capacities of 20 GVA and 500 MVA indicated are unlikely to be encountered in practice, especially with a continuous line section of 500 km between the two ends. However, such a system forms a useful basis of comparison between the performance of the proposed scheme, with that of conventional relays. A unity source impedance ratio ie $Z_{SO}/Z_{SI} = 1$, which is a practical figure, is assumed to ensure that the setting procedure developed in the

previous Chapter is directly relevant to these studies. Moreover, a typical X/R ratio of the sources of 30 is assumed. The following table then gives the appropriate relay constants to be set for the above source capacities for either 50 or 70% series compensation, assuming that in the former case, all compensation is provided at the mid-point and at the line ends for the latter. The line section length between P and Q is 500 km.

	Source Capacity (GVA)	Max external fault current (A, Secondary)	k_i	k_{v2}	D	K
50% Comp	20	2.66	0.965	0.929	4	3
	0.5	0.43	1.561	0.750	2	1
70% Comp	20	4.08	0.777	0.748	4	3
	0.5	0.44	1.554	0.747	2	1

Table 7.1: Relay settings as a function of source capacity and degree of series compensation.

Fault study 1: 3 phase to earth solid fault, location F1 (Fig 7.1a), fault inception at zerocrossing of 'a' phase prefault voltage and 70% series compensation.

This fault condition effectively isolates the two ends, and certain points relating to the performance of the relay at each end may then be discussed separately, as follows.

The primary system waveforms and those corresponding to the different relay stage outputs are given in Figs 7.3 to 7.6. First of all, considering the primary system voltages at end P, Fig 7.3a shows that they collapse to zero after the very rapid by-passing of the end P capacitors. The line currents, as expected, are significantly offset and their magnitudes, by virtue of it being a close up fault, are quite large, as shown by Fig 7.3b. The capacitor voltages at each end are illustrated in Fig 7.4 which clearly shows that whilst the end P capacitor voltages very quickly exceed the threshold level, there is insufficient fault current flowing from end Q to cause capacitor by-passing at that end. The response of the relay R_P is described by Fig 7.5, with Figs 7.5a and b showing the secondary voltages and currents at the relaying point, corresponding to the primary system variations described above. The superimposed modal voltages are illustrated in Fig 7.5c whilst because of the close up fault condition, the rather large relay input current levels are seen to produce distorted outputs from the superimposed component extraction stages (Fig 7.5d). This is due to the fact that the input current levels are significantly larger than those levels upon which the relay settings are based. Consequently, the corresponding voltage produced by the CIM is limited or 'clipped', such that the output of the latter is +/- 10 V maximum. The filtered superimposed voltages fall to zero at approx 55 ms after fault inception (Fig 7.5e), whilst in the current channel, the levels remain quite significant. This situation is tolerable, since this internal fault condition would result in circuit isolation, thus giving the relay a more than adequate period in which to reset. The signals S_1 and S_2,

together with their associated dynamic thresholds (T_2, T_3) become dominated by the residual current component in the subsequent post-fault period as shown in Figs 7.5 g and h. This is to be expected, because the absence of any voltage signal gives $S_1 = -I$ and $S_2 = +I$, resulting in relaying signals which are equal in magnitude, but of the opposite polarity. However, such a situation results in no magnitude and rate of rise differences as indicated by Figs 7.5i and j. There is therefore, an indication that relay recovery could be achieved quickly, but this is not in fact possible as any superimposed quantities generated by a subsequent disturbance would not be reflected in the output of the extraction stages, because of the aforementioned current channel clipping. The detailed waveforms of Figs 7.5k and l clearly show that the initial variations of DM and DR cause rapid up-counting of the bi-directional trip counter (Fig 7.5m), since the polarity of the two functions is the same. This permits ultra-high-speed detection of the fault.

The response of the end Q relay, R_Q is somewhat different to that at end P, with the voltage channel being rather noisy by comparison. As expected, significant travelling wave distortion is evident in the secondary phase and superimposed modal voltages of Figs 7.6a and c respectively. The frequency of these waves is approximately 150 Hz, as expected for the line section length, for which, the averaging stages clearly provide adequate attenuation as shown in Fig 7.6e. The secondary phase currents are shown in Fig 7.6b and because there is no by-passing of the end Q capacitors, subsynchronous currents dominate both the superimposed components of Figs 7.6d and f and the relaying signals S_1 and S_2 (Figs 7.6g and h). Because of the

filtering philosophy adopted, the digital filter does not attenuate such components, but as shown in Figs 7.6g and h, the thresholds T_2 and T_3 are maintained well above S_1 and S_2 for the whole period after T_2 and T_3 begin to rise following fault inception, thus preventing any relay mal-operation. In the presence of subsynchronous currents and hence relaying point subsynchronous voltages, the above feature is essential, since, as observed in Figs 7.6i and j, significant DM and DR is produced, long after fault inception. Hence the latter could result in trip counter operation if the relay is not de-sensitised. This is not so important for the internal fault condition being considered, since as mentioned previously, the internal breakers would be tripped. However, these results highlight the stability of the relay under system resonant conditions as achieved by the dynamic threshold function, this feature being of prime importance for external faults. Considering the detailed responses of Figs 7.6k and l, the forward indication from DM and DR for each mode, enables the trip counter to reach the decisive level in less than 5 ms, as shown in Fig 7.6m. Such a speed of operation is exceptional, since under this condition, the fault is 500 km from end Q and there is a propagation delay of 1.66 ms before the superimposed Aerial mode components arrive at the relaying point from their point of origin, F.

Fault study 2: 'b' phase to earth external fault on busbar Q (point F2, Fig 7.1a), 70% series compensation, fault inception at the peak of the prefault 'b' phase to earth voltage.

The primary system waveforms obtained for this fault condition are shown in Fig 7.7, in which the 'b' phase capacitor flashover times at each end are observed to be almost identical (Fig 7.7a and b). This is so because the line currents are common to both ends for an external fault situation. The faulted phase line currents of Figs 7.7c and d reduce in magnitude very quickly after the capacitors are by-passed, this being a direct result of the step increase in the transfer impedance, of the 'b' phase, between the fault and end P. Because of the relatively 'stiff' busbar at P (high source capacity) and the fact that the fault is 500 km from end P, no significant drop in the faulted phase line voltage is evident in Fig 7.7e, whilst at the faulted end, the line voltage collapses to zero (Fig 7.7f). The corresponding relaying point waveforms are given in Figs 7.8 and 7.9 for which it is recalled that the Karrenbauer Transform is employed to form the modal relaying voltages;

$$V_2 = Va - Vc \quad \text{and} \quad V_3 = Va - Vb$$

For a 'b' to earth fault, equal mutual voltages are ideally developed in the healthy phases, which in this case, would result in no mode 2 signal. Considering first of all relay R_P , the secondary voltages and currents are shown in Figs 7.8a and b, whilst it is evident from Figs 7.8c and d, that only minor noise quantities are present at the voltage and current mode 2 extraction stage outputs, with such quantities being hardly discernable after the filtering stages (Figs 7.8e and f). The maximum amplitude of the mode 2 relaying signals, as shown in Fig 7.8g, is well below the minimum threshold of 40 ql, whilst the corresponding mode 3 signals are very large (Fig 7.8h).

The peak DM is only 8 ql for mode 2 as shown in Fig 7.8i which contrasts the very large corresponding DM and DR variations of mode 3, given in Fig 7.8j. In the first 6 ms post-fault, the detailed waveforms of Figs 7.8k, 1 and m, clearly indicate that no possible decision whether correct or otherwise can be made from the mode 2 measurands. However, high speed fault detection is achieved with the mode 3 signal variations as the relay decision is based upon the first trip counter to reach the decisive level. Now considering the relay R_Q, the secondary voltages and currents are given in Figs 7.9a and b, whilst the mode 2 superimposed voltage of Fig 7.9c is seen to be slightly higher in magnitude than that of the relay R_P, due to imperfect transposition of the line section between end Q and the fault. High frequency components are evident in the mode 2 voltage of Fig 7.9c, but the latter are filtered out quite adequately as shown in Fig 7.9e. Figs 7.9d and f show once again, that the corresponding mode 3 superimposed quantities are very much larger, as expected. As revealed by Fig 7.9i, the peak DM and DR, for mode 2, in the initial fault period, is well below the required level to initiate the decision process, whereas the mode 3 DM and DR are quite significant as shown in Fig 7.9j. The detailed DM and DR variations are given in Figs 7.9k and 1, whilst ultra high speed detection of the external fault is achieved, since as shown in Fig 7.9m, the mode 3 trip counter rapidly decrements to a count of -5. The combined decisions of the relays at each end would then be to inhibit breaker opening on the protected line section, as the directional decisions of the two relays do not agree.

The foregoing studies are associated with faults involving all three phases or just one phase and earth, for a series compensated system, the compensation being provided near the line ends. Although not shown here, the relay performance as found to be completely satisfactory for the other two fault types ie the interphase fault not involving earth and the double phase to earth fault. However, for completeness, the latter fault types form the basis of the fault studies below, for a series compensated system with capacitors located at the midpoint.

7.1.2 Compensation at the Midpoint

Fault study 3: 'b' to 'c' interphase fault, 50% midpoint series compensation, at zero degrees on prefault 'b-c' line voltage. Fault location at 20 km, point F3, from end P (Fig 7.1b).

For this fault condition,the waveforms associated with the relay R_P are given in Fig 7.10, and Figs 7.10a and b clearly show that negligible coupling effects are impressed upon the unfaulted 'a' phase. This is expected, since an ideal interphase fault generates no zero sequence currents and for such a small line section between the point of fault and relay R_P, negligible error due to unsymmetrical tower conductor separation is introduced.

The filtered superimposed modal voltages decay rapidly to zero after fault inception (55 ms approx), as shown in Fig 7.10c and there is no by-passing of the centrally located series capacitors since the fault current from the weak source at end Q is very low. This gives rise

to subsynchronous currents which in turn result in some low level output in the end P current channel for some time after fault inception, thus preventing rapid relay recovery, as shown in Fig 7.10d. The fault is however, internal to the protected zone and correct directional determination which is of primary importance, is achieved with uhs by both modes, as shown by Figs 7.10e, f and g. At end Q, Fig 7.11 clearly shows the travelling wave corruption in the voltage channel and the relatively high prefault steady state currents. The detection process is however unaffected, as indicated by Figs 7.11 e, f and g, despite the post fault input currents being of a similar magnitude to the steady state prefault levels in addition to containing substantial subsynchronous current levels. Such behaviour serves to emphasise the excellence of this protection relay, based upon superimposed components measurement, as a relay measuring from the total signal variations, such as an overcurrent device, could not in a similar situation, discriminate between the normal load condition and the fault condition.

Fault study 4: Double phase to earth fault, involving the 'b' and 'c' phases, fault inception at the peak of the prefault 'b-c' line voltage, close to the centrally located capacitor bank (point F4, Fig 7.1b).

Similar discussion to that for the previous fault study is relevant, but considerable coupling is introduced onto the 'a' phase, since the fault involves earth. Figs 7.12 and 7.13 illustrate the relay responses of R_P and R_Q respectively, with the current channel of relay R_Q undergoing considerable distortion. Again correct high

speed directional indication is achieved at both ends, as shown in Figs 7.12 and 7.13e, f and g.

In comparison to the first two fault studies, in which the line was loaded to a typical level of 1000 MVA, fault studies 3 and 4 included no prefault loading and as such, it is concluded that the presence of any load current does not detract from the high speed capability of the relay. However, loading may influence the magnitude and phase angle of the prefault point voltage, relative to the busbar voltages behind the relay locations, but no significant difference in the superimposed forcing voltage and hence the rate of rise of the relaying point superimposed components would result.

7.2 Overall Relay Performance

For the system of Fig 7.1a, with source capacities of 20 GVA and 500 MVA at P and Q respectively and 70% series compensation, general operating characteristics were determined.

7.2.1 The Influence of Fault Type and Fault Inception Angle Upon Relay Operating Times

Figs 7.14 and 7.15 illustrate the fault type dependency of the operating times of the directional relays R_P and R_Q. For zero degree fault inception angle (fia), Fig 7.14 shows that minimum operating times are achieved under three phase to earth fault conditions and corresponding maximum times for single phase to earth faults. This is expected, since in the former case, the modal signals have significantly greater energy content, for any distance to fault. Moreover, Fig 7.15 illustrates the fault angle dependency upon the operating times for both three phase and single phase to earth faults.

The greater rate of rise of the superimposed signals through the decision process, as generated by fault occurring near the peak of the prefault voltages, results in a rapid increase in the trip counter output. Conversely, a fault occurring near a zerocrossing may be, in the initial period, analysed by the application of a 'ramp' type superimposed generator at the fault point, which results in a more gradual rate of rise in the measurands. Comparing the 0 and 90 degree fia responses, a relatively larger difference in operating times is observed for single phase to earth faults, due to the nature of the modal relaying signals. For an 'a' to earth fault, S_1 and S_2 are dominated by the superimposed 'a' phase quantities, ie for the voltage components alone;

$$S_1 \simeq Va \quad \text{and} \quad S_2 \simeq Va$$

Hence the fault point on wave of the faulted phase directly affects the relaying signal behaviour. However, for the three phase to earth fault case, whilst one phase voltage may be close to a zerocrossing, the other two phases would then be approaching their peaks. In this way, a more constant operating time/fia characteristic is obtained for three phase to earth faults or indeed double phase to earth faults, when compared to that for single phase to earth faults.

The fault point on wave effect upon relay operating times is further illustrated in the polar charts of Figs 7.16 and 7.19. Comparisons are made between the relay responses for both single phase to earth and three phase to earth faults, over the range 0 to 360 degrees.

The circular characteristics of Fig 7.16 emphasise the relatively constant operating time/fia performance for both relays. In general, it is noted that the relay R_p is faster for close up faults, ie a fault at P (x_F = 0 km) is detected by relay R_p quicker than a corresponding fault at Q (x_F = 500 km), detected by relay R_Q. This is explained by the fact that the decision process bases it's decision upon the smallest superimposed component (voltage or current). At P, the smaller component is the superimposed voltage and with a source coverage gain k = 3 at that end, the voltage level relative to the associated current, within the relay R_p, is increased. The response of the relay R_Q however, is governed by the superimposed current because of the relatively weak source connected to busbar Q and as such, no equivalent source coverage gain is introduced.

The corresponding single phase to earth fault results are vastly different with a marked decrease in operating speed for second and fourth quadrant faults (Fig 7.17). This is due to the signal polarity reversal influence as described in Chapter 5, whereby, at low signal levels, there may be a small period in which the trip counter is held constant, below the decisive level. More importantly however, the slowest operating time is approximately 10 ms, which is still very fast. For the relay R_p, Fig 7.17a shows that the difference in operating times between x_F = 0 and x_F = 500 km is significantly greater than that for R_Q for corresponding faults. This is again due to the fact the superimposed voltage presented to R_p , is relatively small when compared with the associated superimposed current. Now with a very low terminating impedance

(20 GVA scl), an increase in the line impedance between relay R_p and the fault, greatly diminishes the magnitude of the end P superimposed voltage component. However, at Q, the very high source impedance ensures that relay operation is governed by the current components, with the line impedance having a less dominating effect upon the latter. Thus a more constant characteristic is obtained at Q for $x_F = 0$ and $x_F = 500$ km, as shown in Figs 7.17. Figs 7.18 and 7.19 further highlight the relay performance at each end for both fault types considered, again emphasising that the slowest operating times are obtained for single phase to earth faults, but even so, guaranteed operation in 10 ms or less is more than adequate to categorise the relay response as high speed.

7.2.2 Relay Performance Studies for a Practical System

Considering the multi-section feeder system of Fig 7.20, the combination of infeeding and local generation behind busbars P and Q, yields effective short circuit levels of 3.75 and 4.0 GVA respectively at the two busbars. With a main line section length of 300 km, 70% series compensation, it is expected that such source capacities would enable significant levels of both superimposed voltage and current to be generated at both relaying points, as the impedances behind the latter are comparable with that of the line. This in turn leads to a faster speed of operation over the range of distance to fault of 0 to 100% from end P, as illustrated in Fig 7.21. In comparison with Fig 7.15, the same general comments are valid, ie three phase to earth faults yield more constant operating times, between 0 and 90 degrees fia (referenced to the 'a'

phase prefault voltage). Faster overall operation is achieved for this system since wave transit times are smaller and less wave attenuation is introduced over the 300 km line as opposed to the previous 500 km feeder. In detail, Fig 7.22 gives the operating time/fia performance of R_P , which for close up faults has a slowest operating time of 5.5 ms. Moreover, an increase in distance to fault does not significantly delay relay operation despite the additional wave transit delay (Fig 7.22b). This serves to illustrate that very remote faults, giving rise to greatly reduced levels of superimposed components and indeed relaying signals, do not cause any significant delay in the performance of the relay proposed. Thus a high degree of sensitivity is achieved with the proposed relay, which is extremely beneficial for the rapid detection of highly resistive faults. Fig 7.23 displays the operating time against fault position characteristic, for both relays, for fault path resistances up to 500 ohms. The high speed performance underlines the advantage of utilising directional, superimposed component relays as opposed to distance schemes for applications where high resistance faults are commonplace. A 500 ohm fault loop impedance would probably be beyond the capability of an impedance measuring device, whereas a coordinated decision of two high speed directional relays, would ensure rapid fault detection.

The foregoing results underline that when applied to a typical series compensated system, the new scheme is extremely reliable and offers high speed performance, over the entire range of fault inception angles and distance to fault, regardless of fault type, in the presence of very high fault path resistances.

Although not shown here, a similar system employing 50% series compensation at the midpoint of the main line section was studied in depth, with similar results and conclusions to those above being obtained regarding the overall relay performance.

In summary, the above typical studies clearly illustrate the fundamental principles of the proposed relay, which as shown, offers total reliability in terms of correctly indicating the direction to fault. The following desirable features have been highlighted;

1) High speed internal and external fault detection.

2) Correct directional determination, with or without series capacitor by-passing.

3) Correct directional determination, with or without prefault line loading.

4) Correct operation under current channel clipping conditions.

5) Stability in the presence of subsynchronous resonance.

6) Operation when a fault fails to generate one of the independent mode signals (ie operation is fault type independent).

7) Operation independence upon both the degree of series compensation being employed and the location of the capacitor banks.

8) High speed fault detection for both very high and very low equivalent source short circuit levels.

7.3 Capacitive Fault Currents

Impedance relays may suffer loss of directional discrimination when series capacitors remain in circuit for the duration of the fault [10]. With reference to Fig 7.24, with low source capacities at R and P, such that no capacitor gap flashover occurs, a fault at F may be detected as reverse to the relay R1 (caused by the line current leading the relaying point voltage), or as a forward fault by the relay R2. In both cases, mal-operation would ensue. However, for superimposed component relays, Fig 7.25 shows that both relays are effectively examining an inductive source, with a superimposed forcing generator located at F. The secondary voltages and currents presented to relay R1, for an 'a' phase to earth fault at F (90 degree fia) are given in Fig 7.26a and b. The large degree of subsynchronous modulation is the dominant feature of the faulted phase waveforms, and because there is only a very small infeed at P, the voltage and current are almost identical for both relays. The polarity of current measurement for R2 is however, opposite to that of R1, and the detailed responses of Figs 7.26c to f clearly show that reliable direction to fault indication is achieved by both relays, that is R1 detects a forward fault and R2 reverse, as expected.

7.4 Capacitor Reinsertion Effects

For the practical system of Fig 7.20, two types of external fault were simulated at F. The first, a three phase to earth solid fault, occurring at the zerocrossing of the prefault 'a' phase to earth

voltage. The fault study included capacitor bank protection with all damping elements omitted, in order that the most severe switching transients would be introduced into the waveforms. At F, Fig 7.27a shows the primary system voltages which simultaneously collapse to zero upon fault inception at time $t = T_F$. The equivalent fault path currents, ie the line currents flowing through circuit breaker B are given in Fig 27.7b and sequential pole opening, approx 1 cycle after fault inception, effectively isolates the faulted section from the main system. The capacitor bank waveforms are given in Fig 7.27c with rapid by-passing of all three individual phase capacitors being evident. After time $t = T_{FB}$, the rest of the system is energised, since the main line circuit breakers would remain closed for the external fault condition, and as such, the by-passed capacitors must be reinserted to regain normal quiescent conditions. At time $t = T_R$, all capacitors are simultaneously reinserted, which causes a notable change in the line voltages and currents, observed in the secondary waveforms of Figs 7.28a and b, at the relay location near busbar P. Under normal circumstances, one would expect a significant current change without an associated change in the voltage, but because the rest of the system is disconnected when B is opened, a very weak infeed with corresponding high impedance is left connected behind busbar P. Hence the superimposed component waveforms of Figs 7.28c to f clearly show finite changes in the relaying point voltages and currents due to reinsertion. The mode 2 relaying signal variations are given in Fig 7.28g and h, in which the threshold T_2 falls to its minimum of 40 ql before reinsertion takes place. Hence full

sensitivity is regained and the detailed DM and DR variations of Fig 7.28i result in a forward disturbance detection, since the trip counter output, displayed in Fig 7.28j reaches the +ve decisive level. Such behaviour is not incorrect since the origin of the disturbance is in the forward direction with respect to relay R_P, but undesirable since unnecessary internal breaker opening would ensue. The results have shown that the relay R_Q does not under these circumstances, detect a forward disturbance, since the relatively high scl at that end does not permit a significant superimposed voltage to be developed, which suggests that for any system with an appreciable infeed at either end, no problems would manifest from series capacitor reinsertion.

In order to counteract the foregoing drawback, a trade off between fault coverage and speed must be weighed against reliable and secure relay operation. The setting procedure adopted, maximises coverage for any given system, with the proviso that large extremes of source capacity and line lengths must be covered. In short, the relay must be de-sensitised to ensure that unnecessary breaker action does not proceed capacitor reinsertion, whilst retaining adequate fault coverage for the application being considered. In this instance, with the minimum threshold increased to 95 ql, a positive trip count of only 1 is obtained, before the dynamic threshold increase, as shown in Fig 7.28k. It must be emphasised however, that the foregoing resultsapply to absolute worst case conditions, ie in the unlikely case of no damping elements being included in the capacitor protections.

A more realistic evaluation of the reinsertion effects is gained by including damping elements which accompany all series capacitor protection schemes. For an 'a' phase to earth fault at F, fault instant at a zerocrossing of the prefault 'a' phase voltage, Fig 7.29a shows the behaviour of the mode 2 relaying signals following the reinsertion of the faulted phase capacitors. A DGS is employed in the capacitor protection. The detailed variations of DM and DR then cause the trip counter output (Fig 7.29e), to once again, attain a +ve count of 5 and as such, the relay detects the reinsertion as a forward disturbance. However, by increasing the minimum threshold to only 65 ql, Fig 7.29f shows that no such counting occurs, with the initial fault detection being unaffected. The effect of increasing the minimum threshold to 95 ql would necessitate an increase in K at the high scl end to 5 instead of 3, but at the low scl end, insufficient current would flow unless that scl was increased to approximately 2.2 GVA. However, should a minimum threshold of 65 ql be taken, a scl of only 1.12 GVA would be sufficient to guarantee relay operation. In comparison, the results obtained for a DGNS are substantially different (Figs 7.29b) to those associated with the DGS. A minor change in relaying signals is observed, which as shown in Fig 7.27d, produces reduced changes in DM and DR when compared with the corresponding DGS results of Fig 7.27c. Even with a minimum threshold of 40 ql, the DM and DR variations for the DGNS case do not initiate any post-reinsertion trip counter action.

These results therefore clearly show that the DGS can, in some cases, cause directional relays of the type proposed to operate following capacitor reinsertion, ie to initiate circuit breaker opening as if an internal fault had occurred. However, the use of the DGNS ensures that the switching transients caused by capacitor reinsertion are so insignificant that de-sensitising the relay to ensure stability for the foregoing sequence of events, is entirely unnecessary. Hence the DGNS not only offers benefits in terms of system stability as fully described in Chapter 3, but also it removes one of the longstanding capacitor reinsertion problems encountered with protection relays applied to series compensated lines.

7.5 Relay Performance for Double Circuit Systems

A major protection problem encountered with double circuit series compensated lines is the effect of the fault position and source configurations, when the capacitors remain in circuit for the duration of the fault. This may lead to voltage and/or current inversion at the relaying points, a specific example of which is dealt with in some detail by Elkateb and Cheetham [10]. The system of Fig 7.2a, with 70% series compensation and no capacitor protection simulation, was studied for a three phase to earth fault on circuit 1, on the line side of the capacitor bank at Q (point F5). The sources behind P and Q were such that the equivalent impedance at Q was many times greater than that at P. Waveforms pertaining to this study are given in Fig 7.30. Because no capacitor by-passing is included, the build up of subsynchronous components is clearly evident in Figs 7.30a

and b, which describe the input voltages and currents to relay R1. It is explained in Reference 10 how under steady state fault conditions, the net effect of the capacitor/line/source impedance combination causes a distance relay at location R1 to lose discrimination. However, this major drawback is overcome by the proposed directional comparison relay at that location, measuring from superimposed components immediately after the occurrence of the fault. Figs 7.30e to 1 show the DM, DR and trip counter responses for the above fault condition, with R1 and R2 on the faulted circuit, correctly indicating an internal fault. Once again however, the coordinated decision of relays R3 and R4 on circuit 2 is to block any breaker action on the latter.

The relay performance was studied for the double circuit systems of Fig 7.2a (50% midpoint compensation) and Fig 7.2b (70% compensation, 35% at each end). With the exclusion of any capacitor protection equipment in the digital simulation, the gain k_i was based on a fully offset through fault current, which in turn yields pessimistic operating times, ie the relay is slightly de-sensitised.

In all respects, the relay performance concerning the fault angle, fault type, distance to fault effects, etc, as described for the single circuit systems, was found to be very similar for the double circuit systems. As such, repetition is avoided in this section, by including only those important results to emphasise the suitability of the relays for double circuit protection.

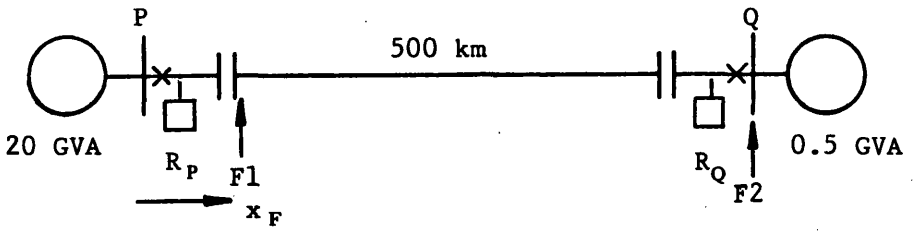
In Chapter 2, it was explained how the use of Aerial mode signals alone, leads to the advantage that, where parallel circuits are involved, it is possible to protect each circuit independently of each other. The relaying point locations, suitable for the protection of the double circuit systems, are indicated by R1, R2, R3 and R4 in Fig 7.2. Figs 7.31 and 7.32 show the relay performance as a function of fault distance (from end P), for a 'b' phase to earth fault on circuit 1. It should be mentioned that a fia of 135 degrees has been chosen, since this produces the slowest operating times on average. For relays R1 and R2, the normal characteristic is obtained, ie the greater fault distances cause slowest relay operation. However, the relays monitoring the healthy circuit yield vastly different responses. Such is the magnitude and direction of the fault current at the terminations, that R3 initially indicates a reverse fault for faults up to approx 40 km from P. Relay R4 on the other hand, indicates a forward fault, but the overall action of the unit protection scheme would be to inhibit breaker opening on circuit 2, whilst R1 and R2 would result in the fault being cleared by the circuit 1 breakers opening. As the distance to fault increases, R4 traverses a very small period of no operation or 'null' region, until it produces a reverse decision. Sometime later, R3 behaves in a similar manner, but the change of direction is from reverse to forward. At no time was there found to be a fault condition which resulted in failure to indicate an external fault by R3 and R4 working as a unit protection scheme. For many other source capacities and various impedance ratios, similar behaviour was observed. Moreover, for other fault types, involving earth or

otherwise, and for faults on circuit 2, the relays R1 and R2 behaved in a similar fashion.

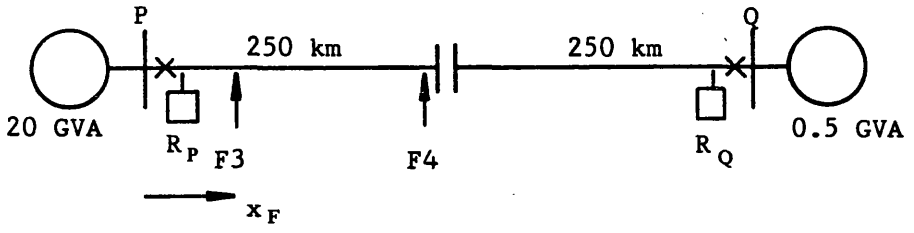
It was therefore concluded that double circuit series compensated lines, or indeed plain feeders, may be adequately protected by relaying each circuit independently, and that new protection relays of the type proposed herein go a long way in overcoming longstanding problems associated with conventional protections.

7.5.1 Intercircuit Fault Relaying

Although not included here, preliminary fault studies were carried out for the same relay configurations as above, for faults involving both circuits, for example a 'b' phase circuit 1 to 'c' phase circuit 2 fault. In this instance the decoupled Aerial mode paths, which have previously enabled independent circuit relaying are interrupted. As such, the preliminary results revealed that direction to fault indication cannot be reliably obtained from all four relays. Further investigation is therefore warranted if the extremely unlikely case of intercircuit fault coverage is required.

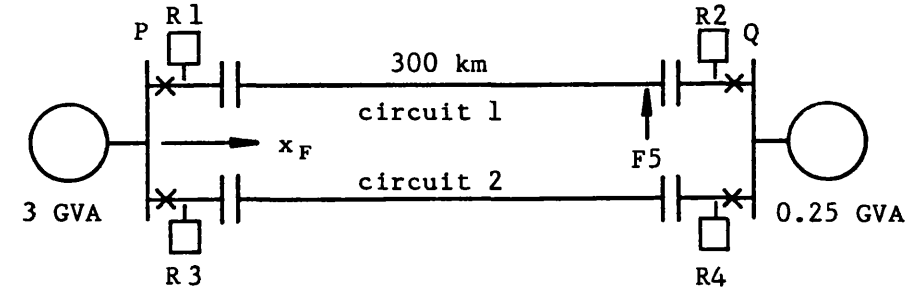


(a) 70% Series compensation

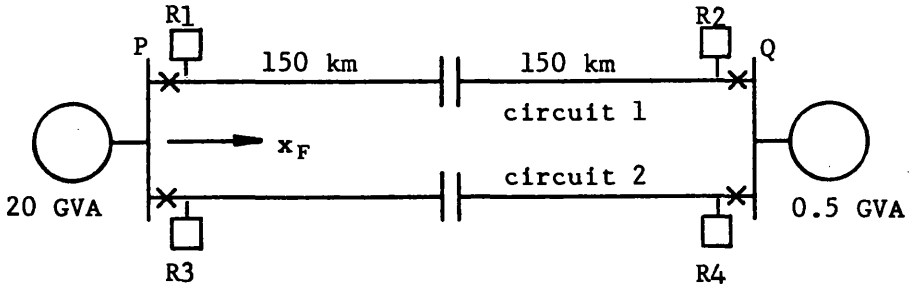


(b) 50% Series compensation

Fig 7.1 Single circuit systems studied



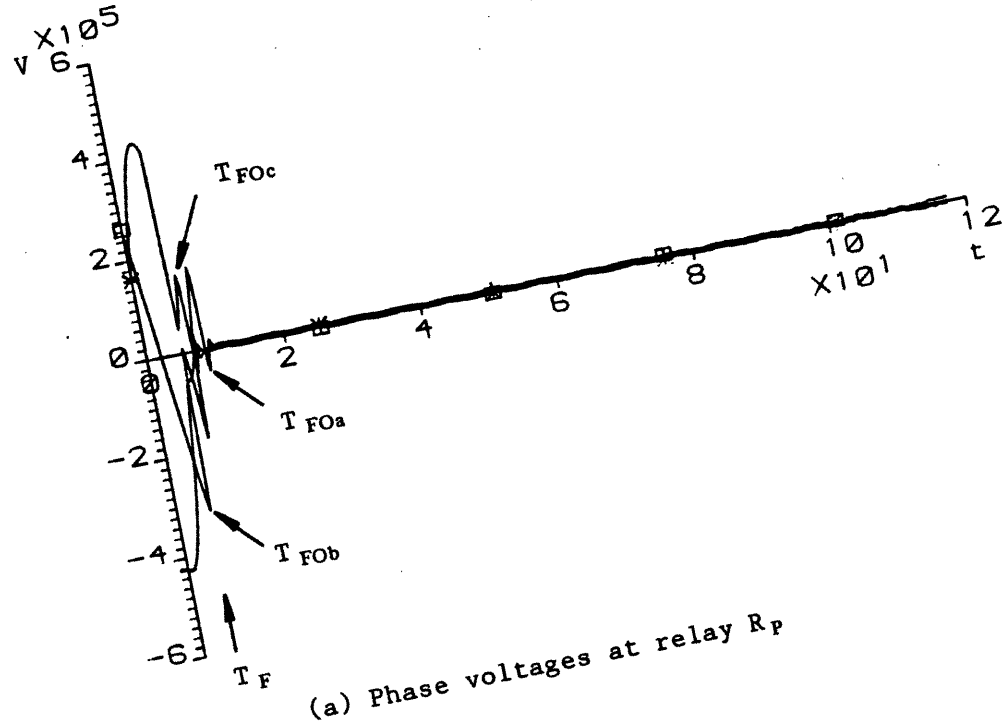
(a) 70% Series compensation



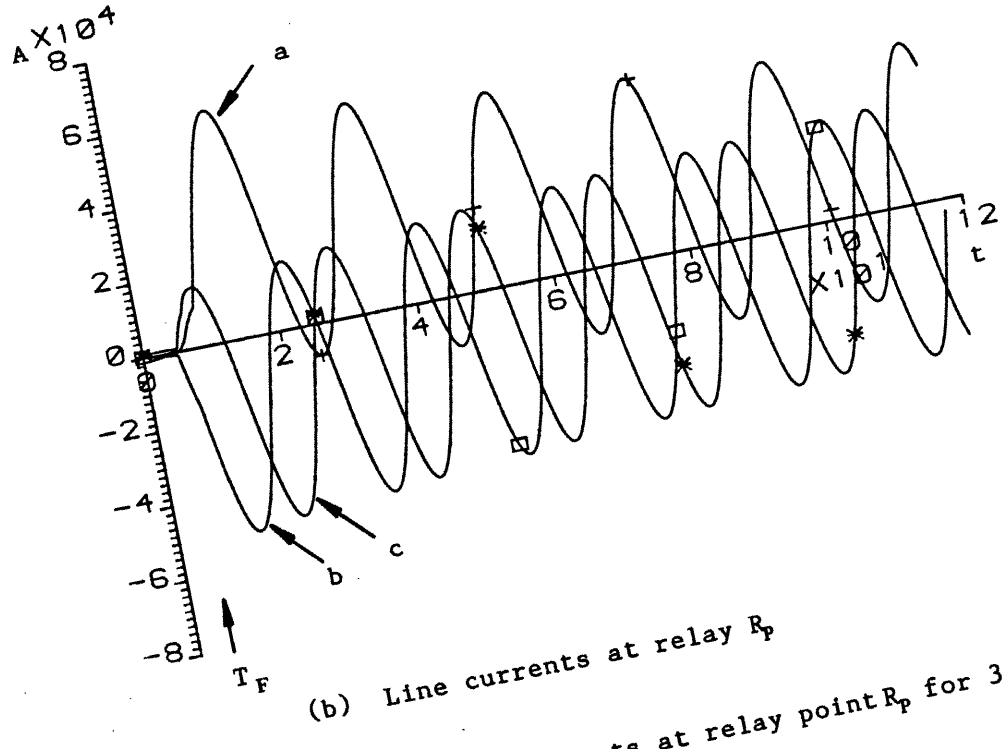
(b) 50% Series compensation

Fig 7.2 Double circuit systems studied

All sources, Z_{SO}/Z_{S1} = 1, X/R = 30

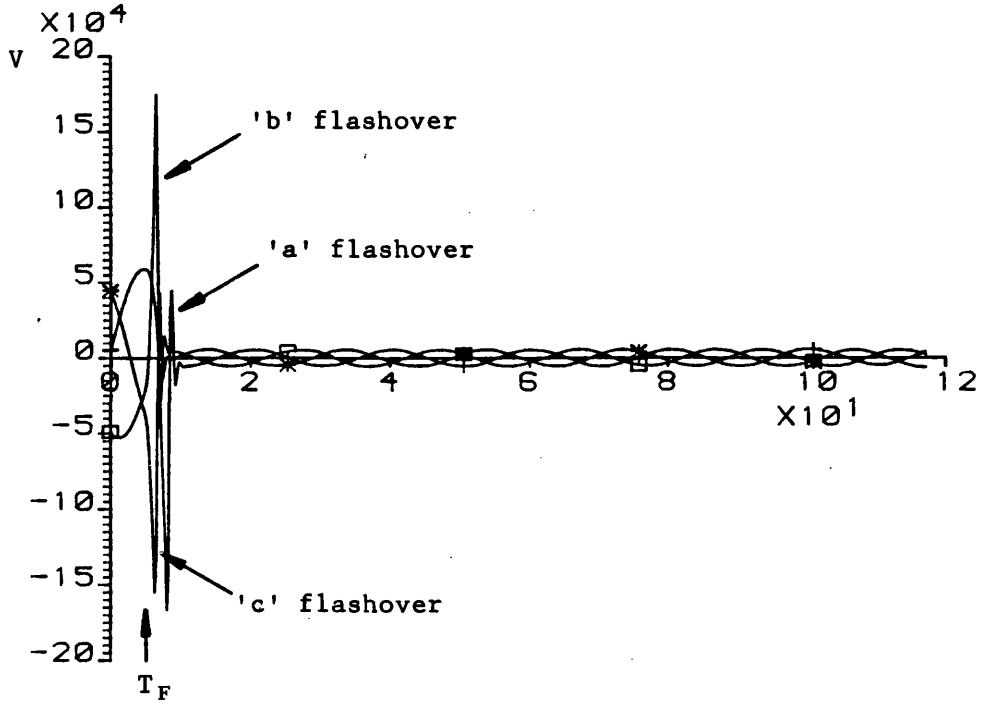


(a) Phase voltages at relay R_P

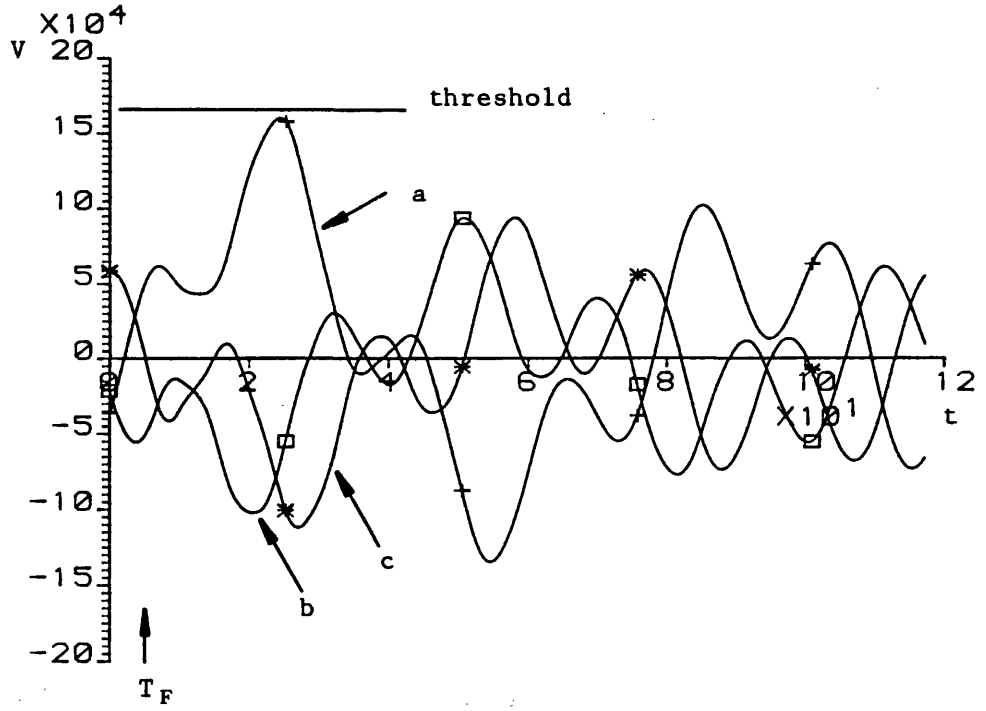


(b) Line currents at relay R_P

Fig 7.3 Primary voltages and currents at relay point R_P for 3 phase to earth fault



(a) End P capacitor voltages



(b) End Q capacitor voltages

Fig 7.4 Capacitor bank voltage waveforms for 3 phase to earth fault

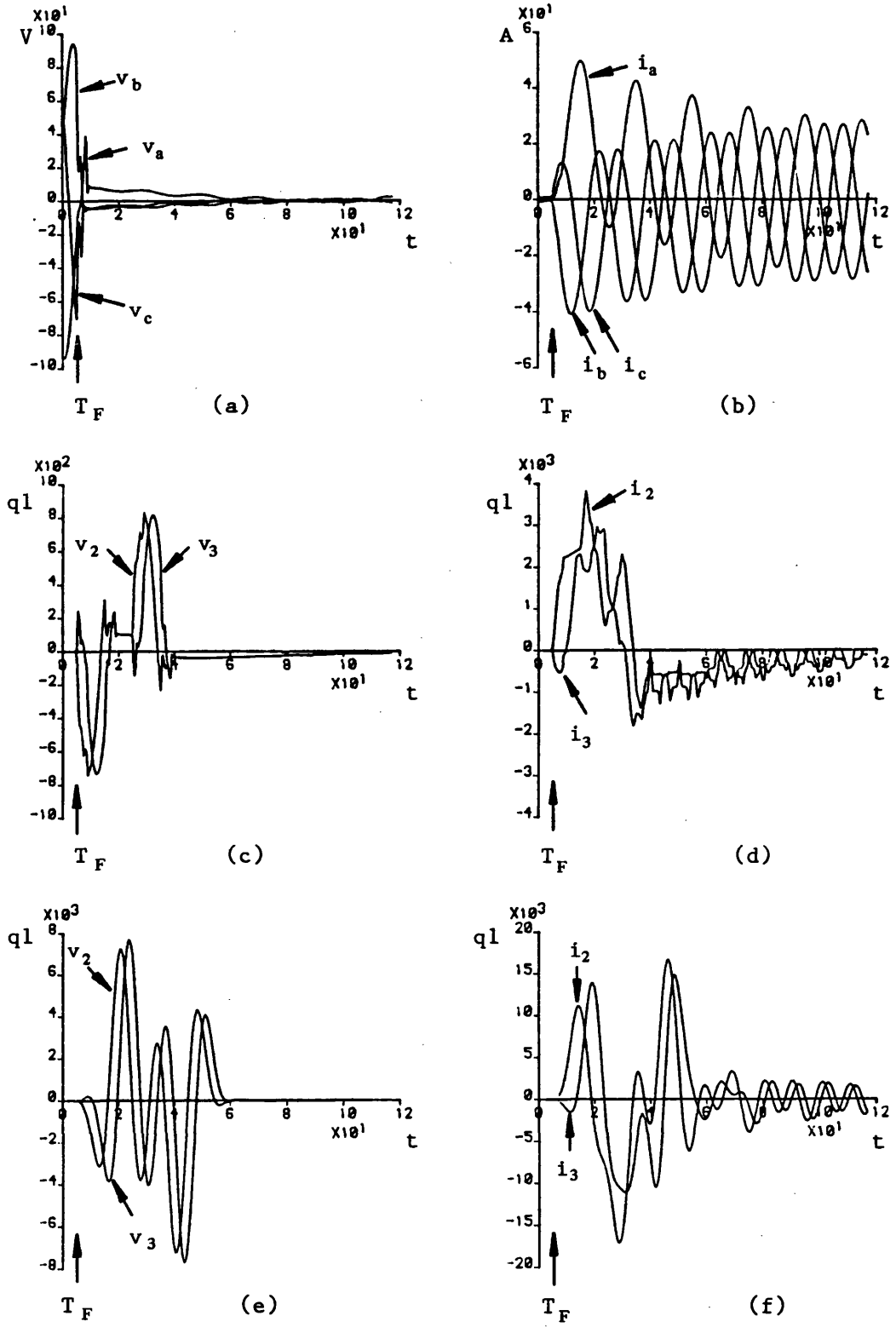


Fig 7.5 Signal variations within relay R_p for 3 phase to earth fault

(a) Pre-filtered voltages (b) Pre-filtered currents

(c) Superimposed modal voltages (d) Superimposed modal currents

(e) and (f) Filtered, superimposed modal voltages and currents

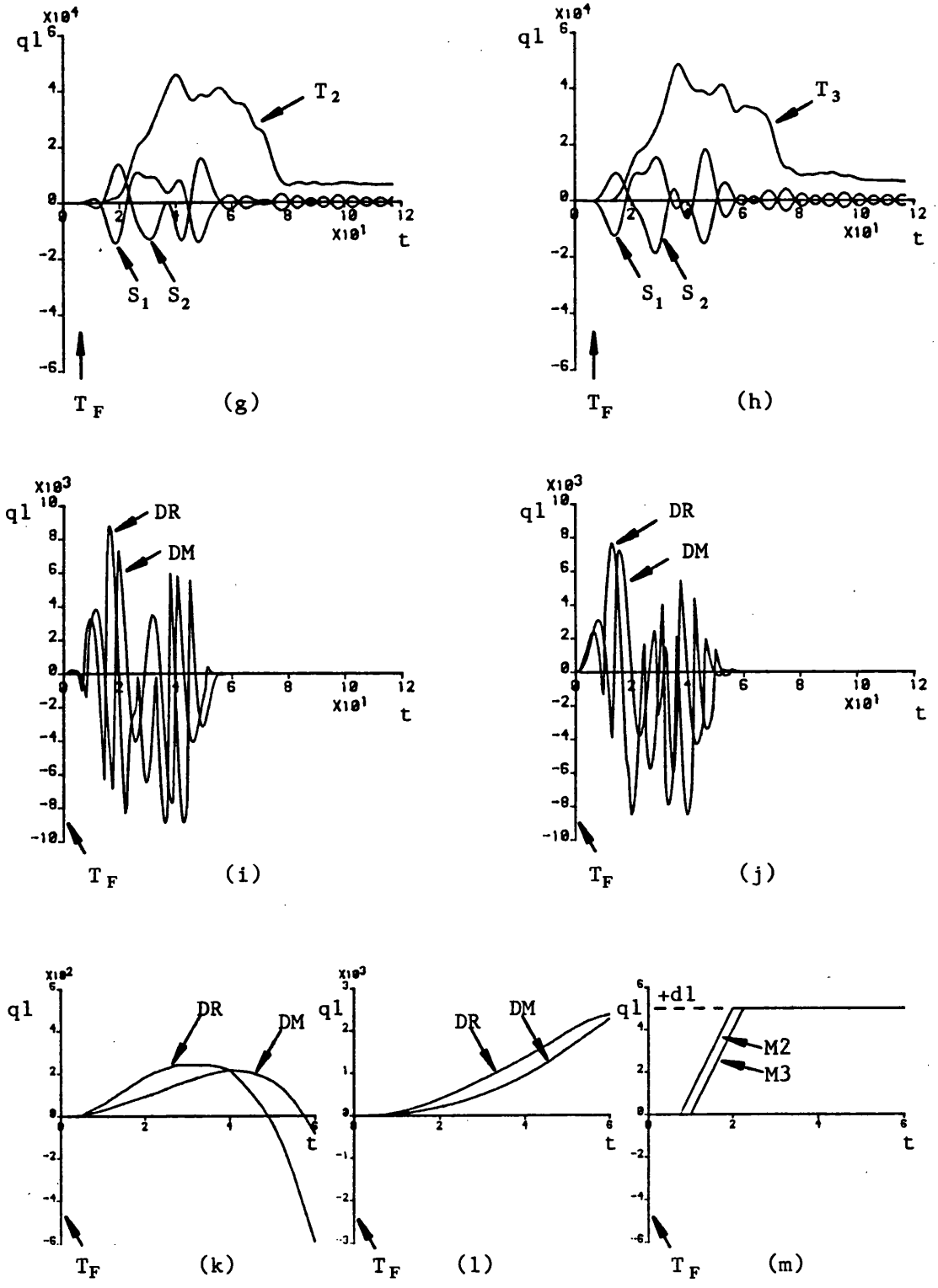


Fig 7.5 Cont'd

(g) M2 and (h) M3 relaying signal responses

(i) M2 and (j) M3 DM and DR variations

(k) M2 and (1) M3 detailed DM and DR variations

(m) M2 and M3 trip counter outputs

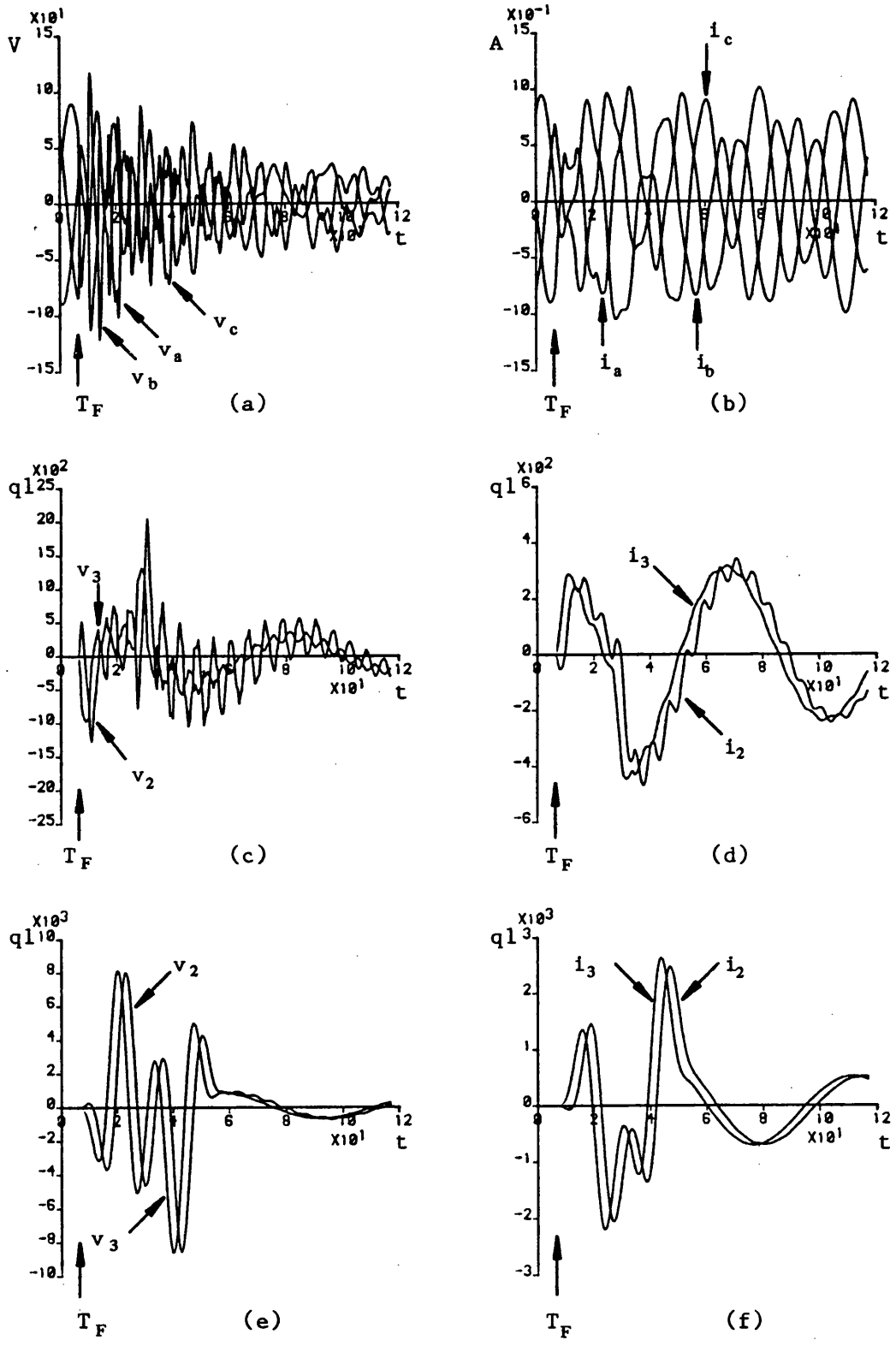


Fig 7.6 Signal variations within relay R_Q for 3 phase to earth fault

(a) and (b) Prefiltered voltages and currents

(c) and (d) Superimposed modal voltages and currents

(e) and (f) Filtered, Superimposed modal voltages and currents

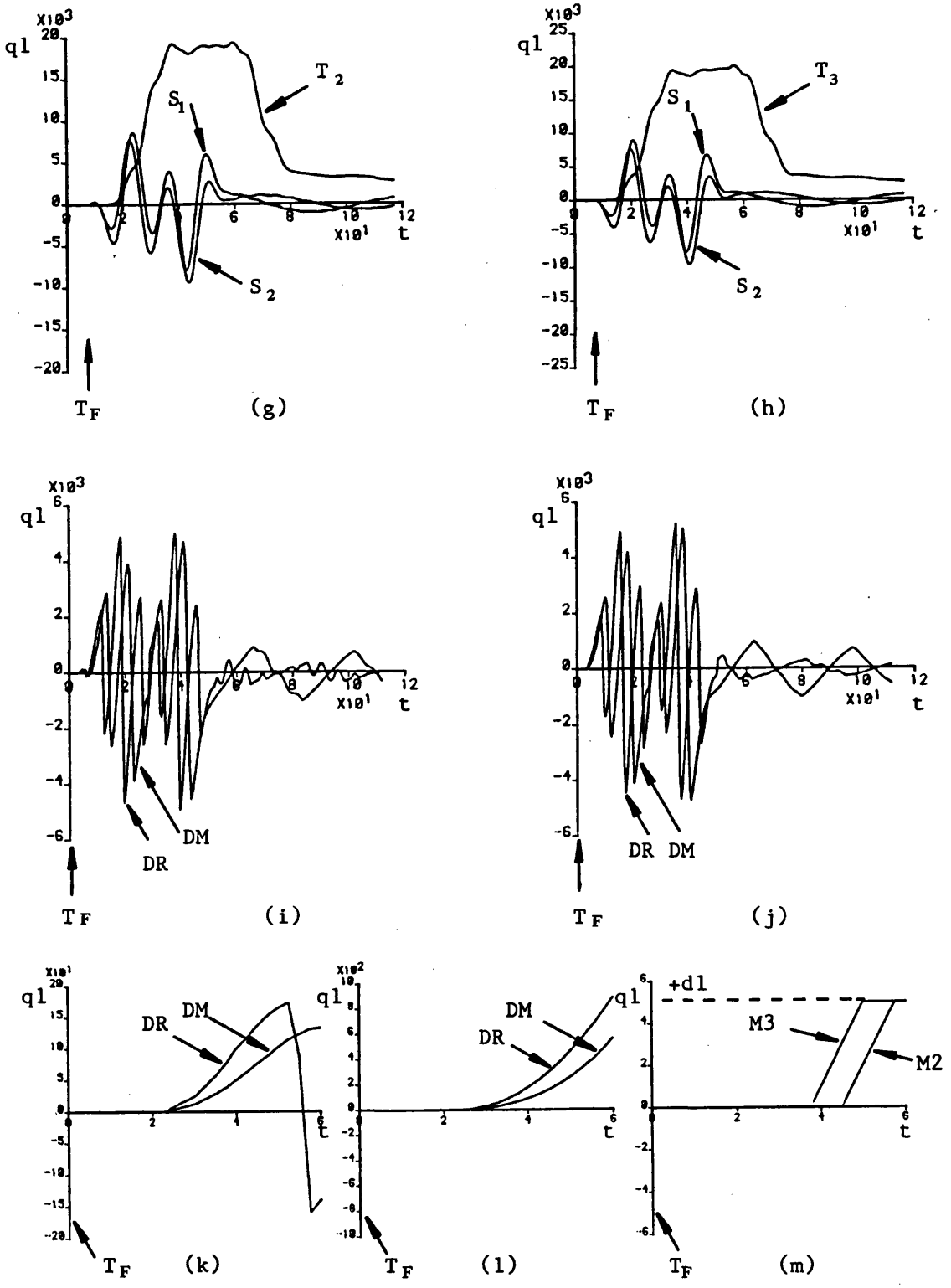


Fig 7.6 cont'd

(g) M2 and (h) M3 relaying signal responses

(i) M2 and (j) M3 DM and DR variations

(k) M2 and (l) M3 detailed DM and DR variations

(m) Trip counter outputs

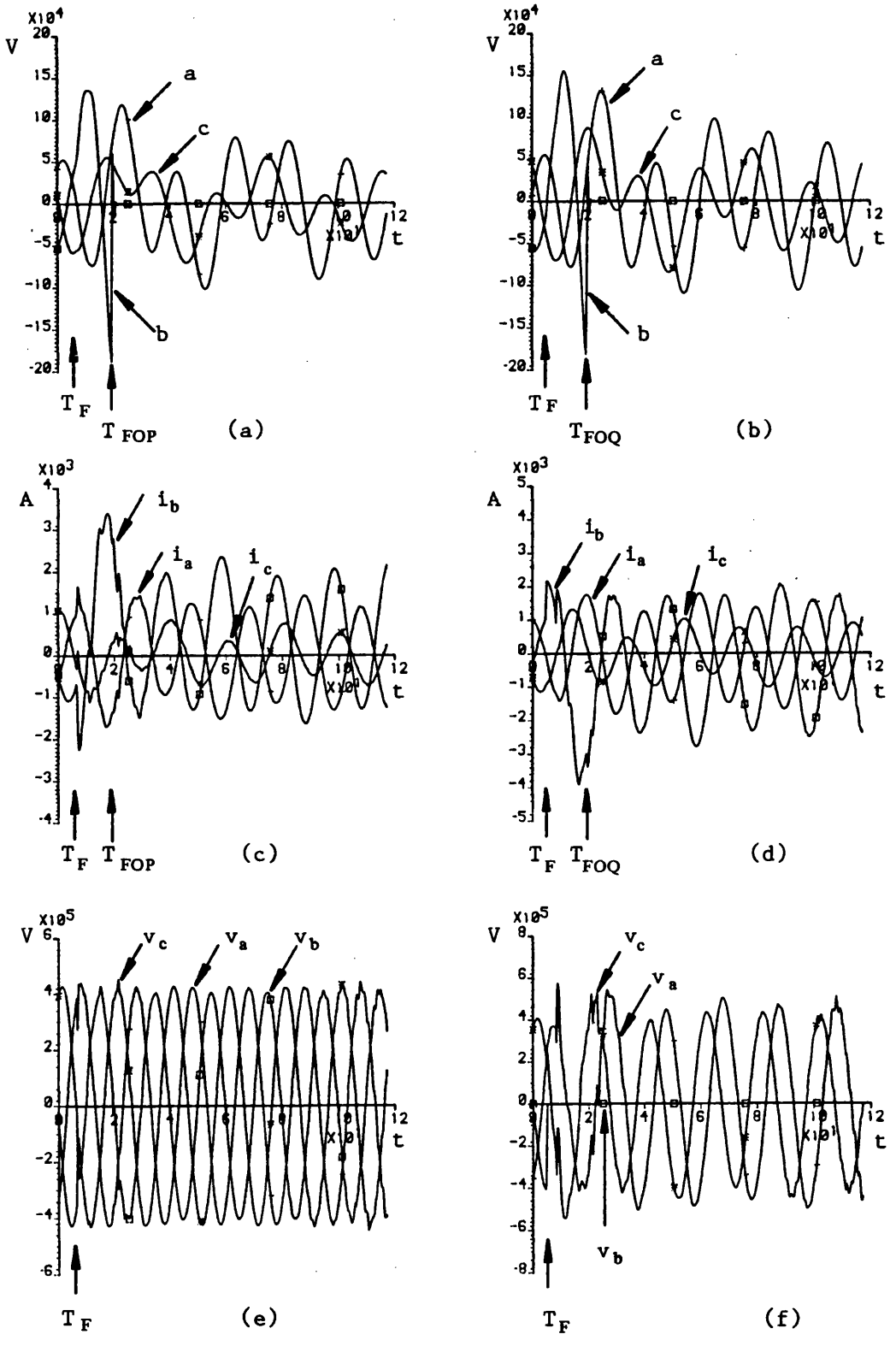


Fig 7.7 Primary system waveforms for 'b' phase to earth fault on busbar Q

(a) End P capacitor voltages (b) End Q capacitor voltages
(c) End P line currents (d) End Q line currents
(e) End P phase voltages (f) End Q phase voltages

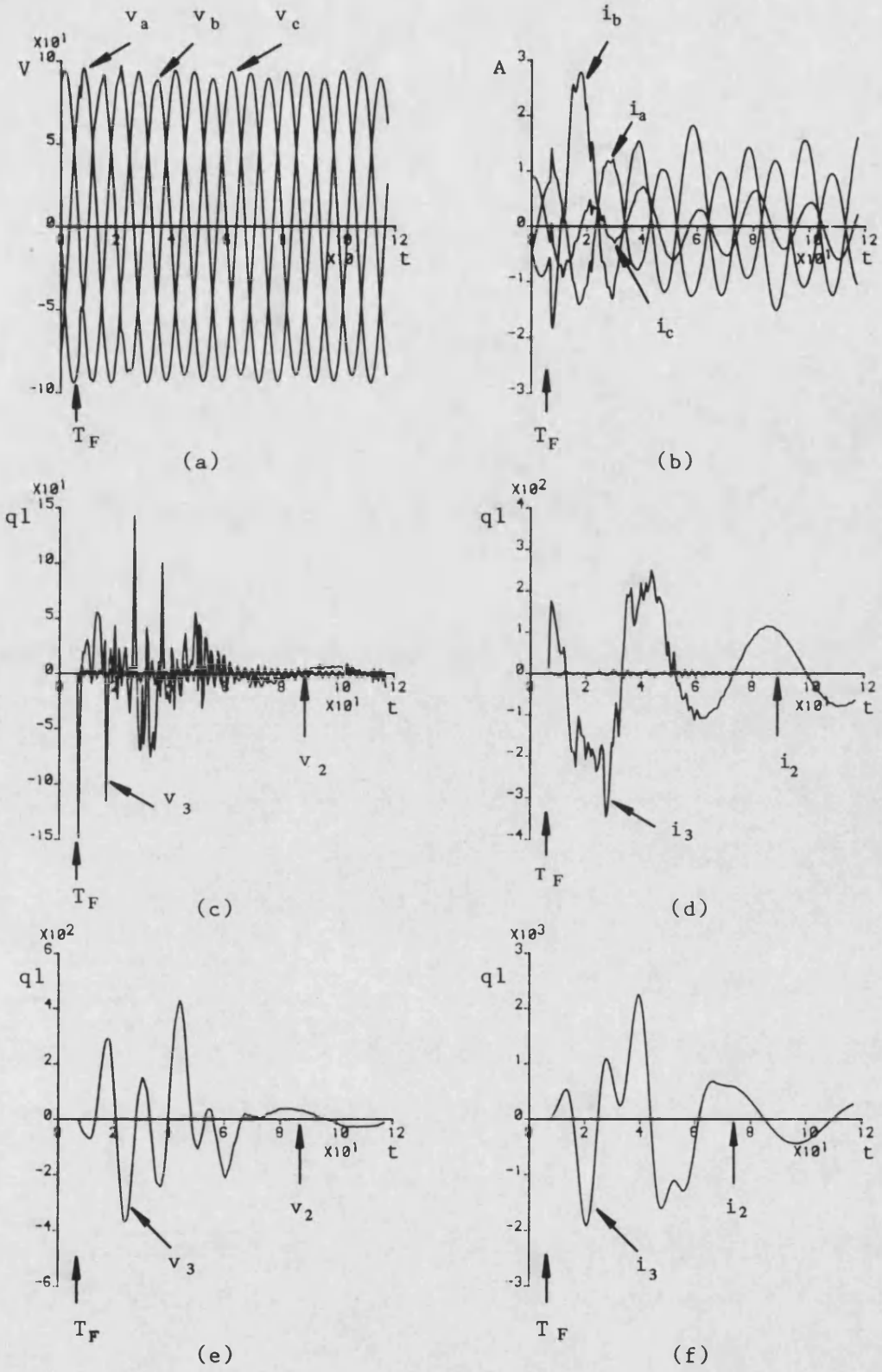


Fig 7.8 Signal variations within relay R_P for 'b' phase to earth fault on busbar Q

(a) and (b) Pre-filtered input voltages and currents

(c) and (d) Superimposed M2 and M3 voltages and currents

(e) and (f) Filtered forms of (c) and (d)

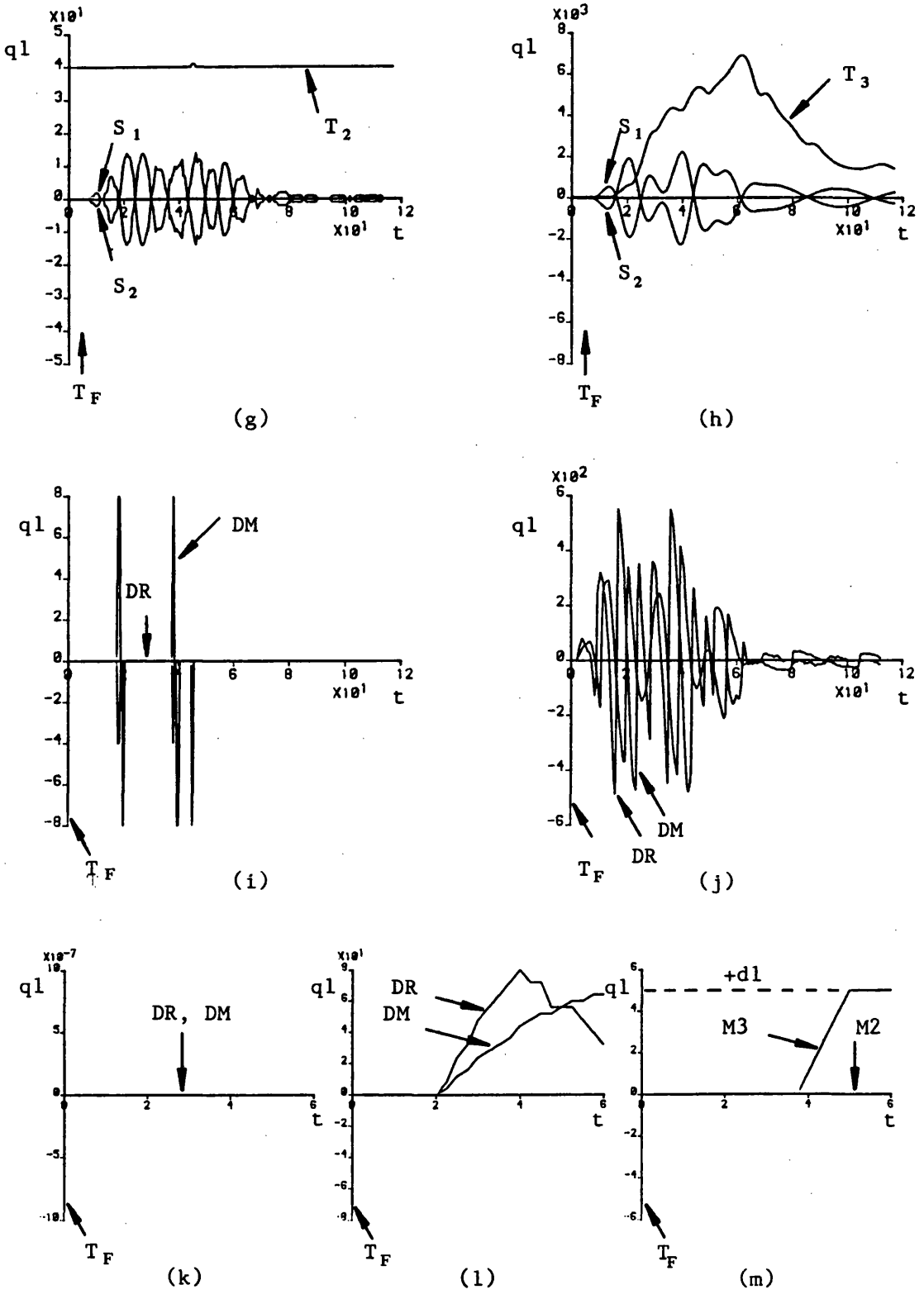


Fig 7.8 Cont'd

(g) M2 and (h) M3 relaying signal responses

(i) M2 and (j) M3 DM and DR responses

(k) M2 and (l) M3 detailed DM and DR responses

(m) Trip counter outputs

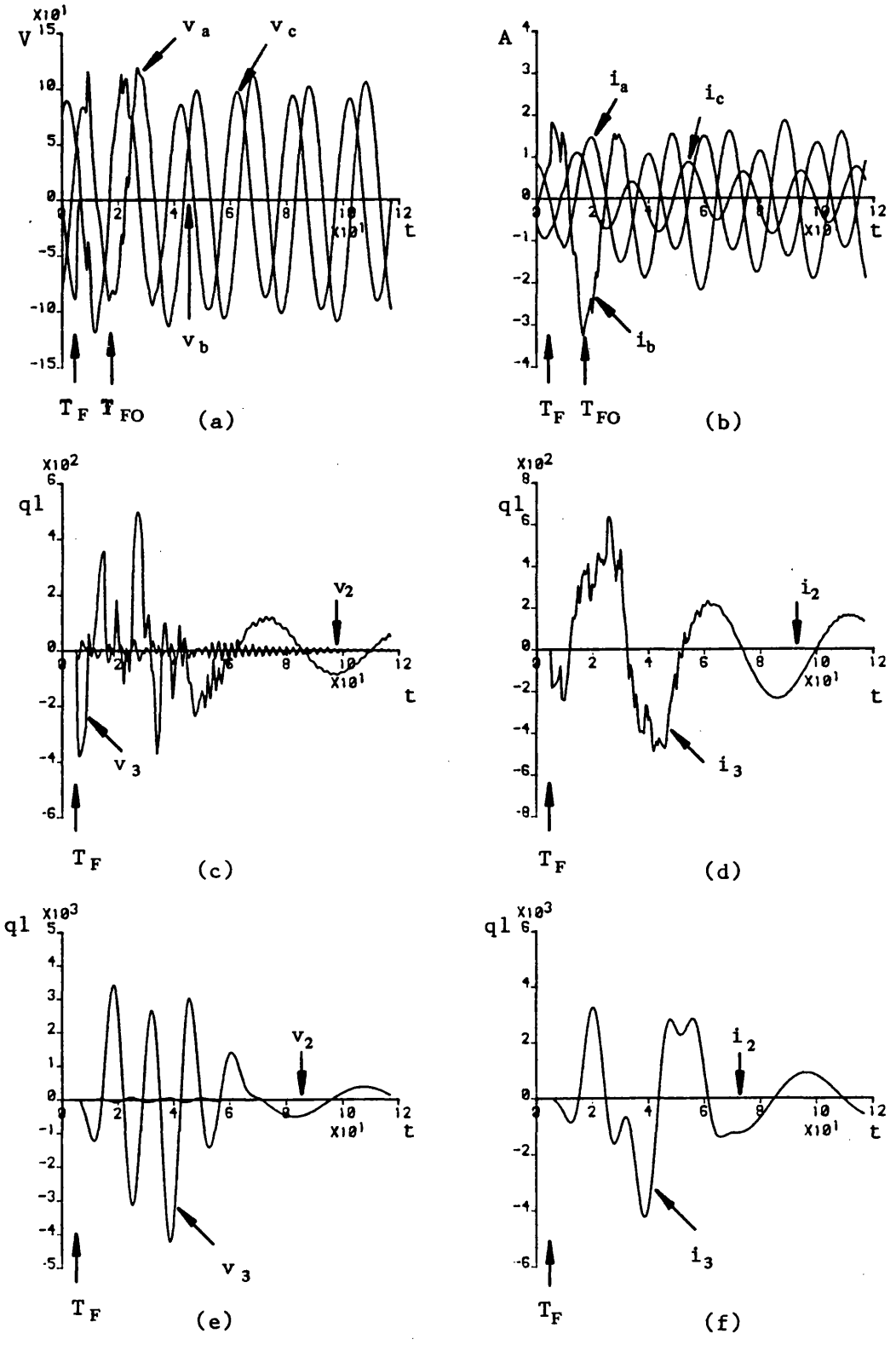


Fig 7.9 Signal variations within relay R_Q, for 'b' phase to earth fault on busbar Q

(a) and (b) Pre-filtered input voltages and currents

(c) and (d) Superimposed M2 and M3 voltages and currents

(e) and (f) Filtered forms of (c) and (d)

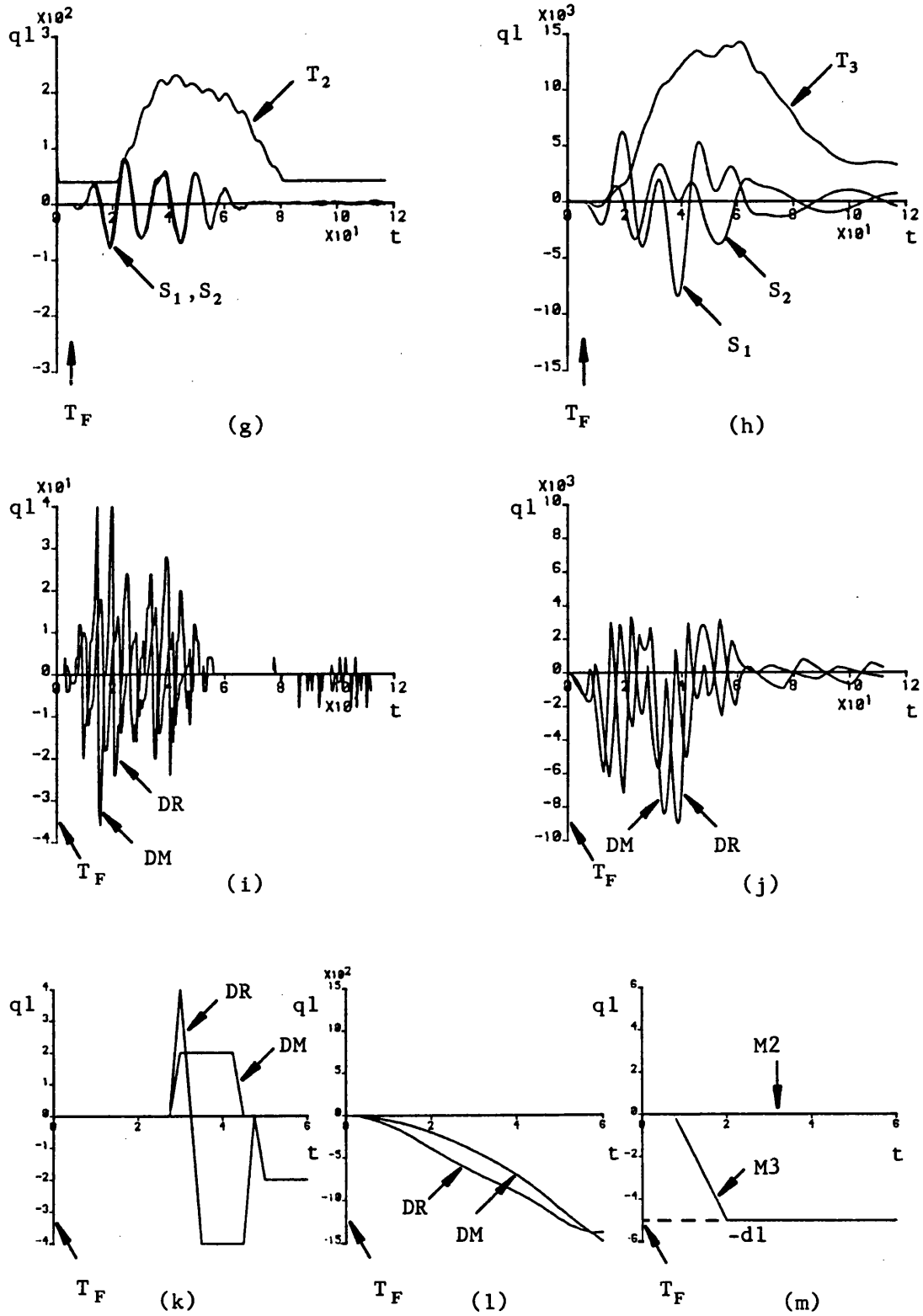


Fig 7.9 cont'd

(g) M2 and (h) M3 relaying signal responses

(i) M2 and (j) M3 DM and DR responses

(k) M2 and (l) M3 detailed DM and DR responses

(m) Trip counter outputs

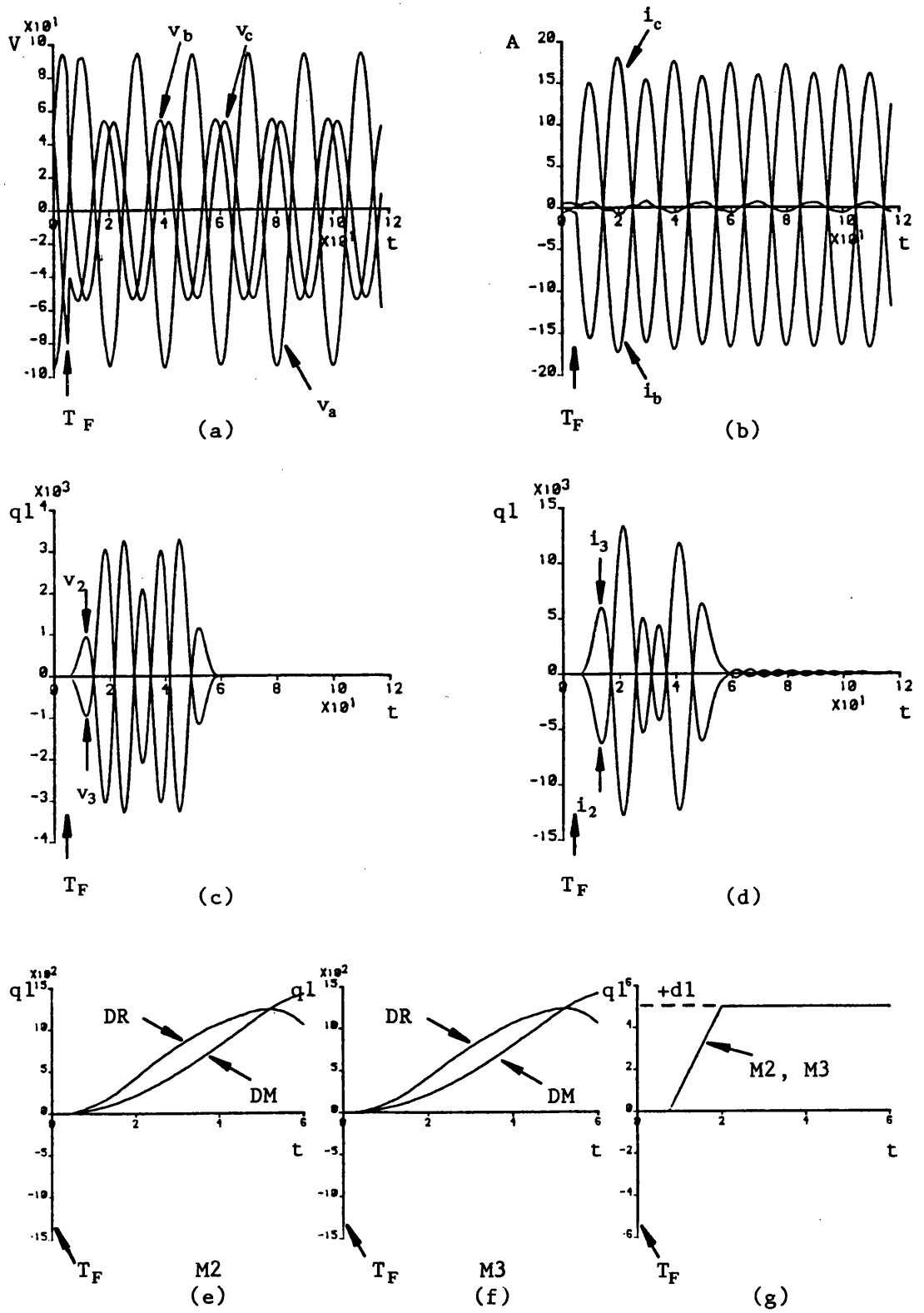


Fig 7.10 Waveforms at various stages within relay at P for 'b' to 'c' interphase fault

(a) and (b) Pre-filtered relay input voltages and currents

(c) and (d) Filtered, superimposed modal voltages and currents

(e) and (f) M2 and M3 detailed DM and DR responses

(g) Trip counter outputs

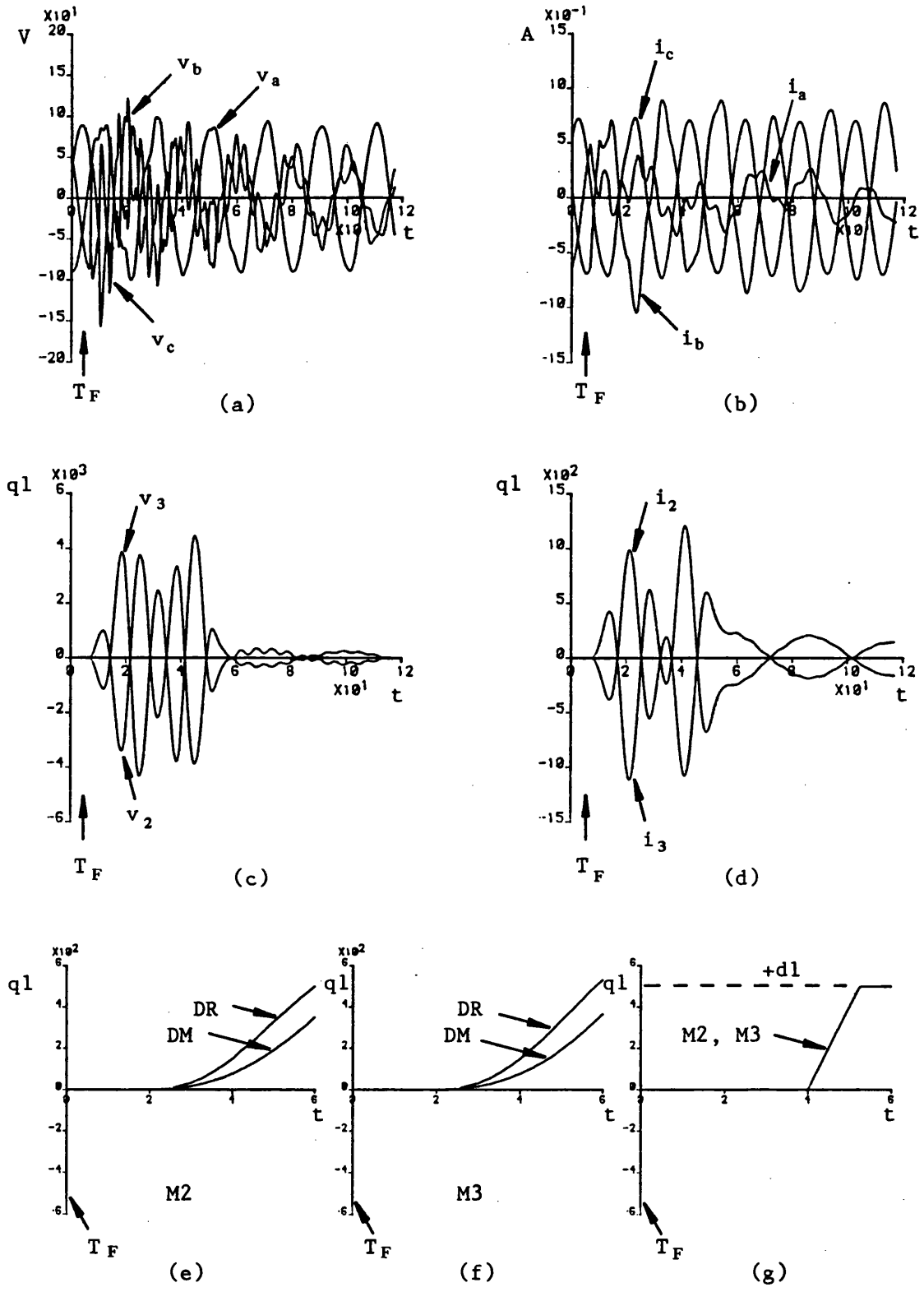


Fig 7.11 Waveforms at various stages within relay at Q for 'b' to 'c' interphase fault

(a) and (b) Pre-filtered input voltages and currents

(c) and (d) Filtered, superimposed modal voltages and currents

(e) and (f) M2 and M3 detailed, DM and DR responses

(g) Trip counter outputs

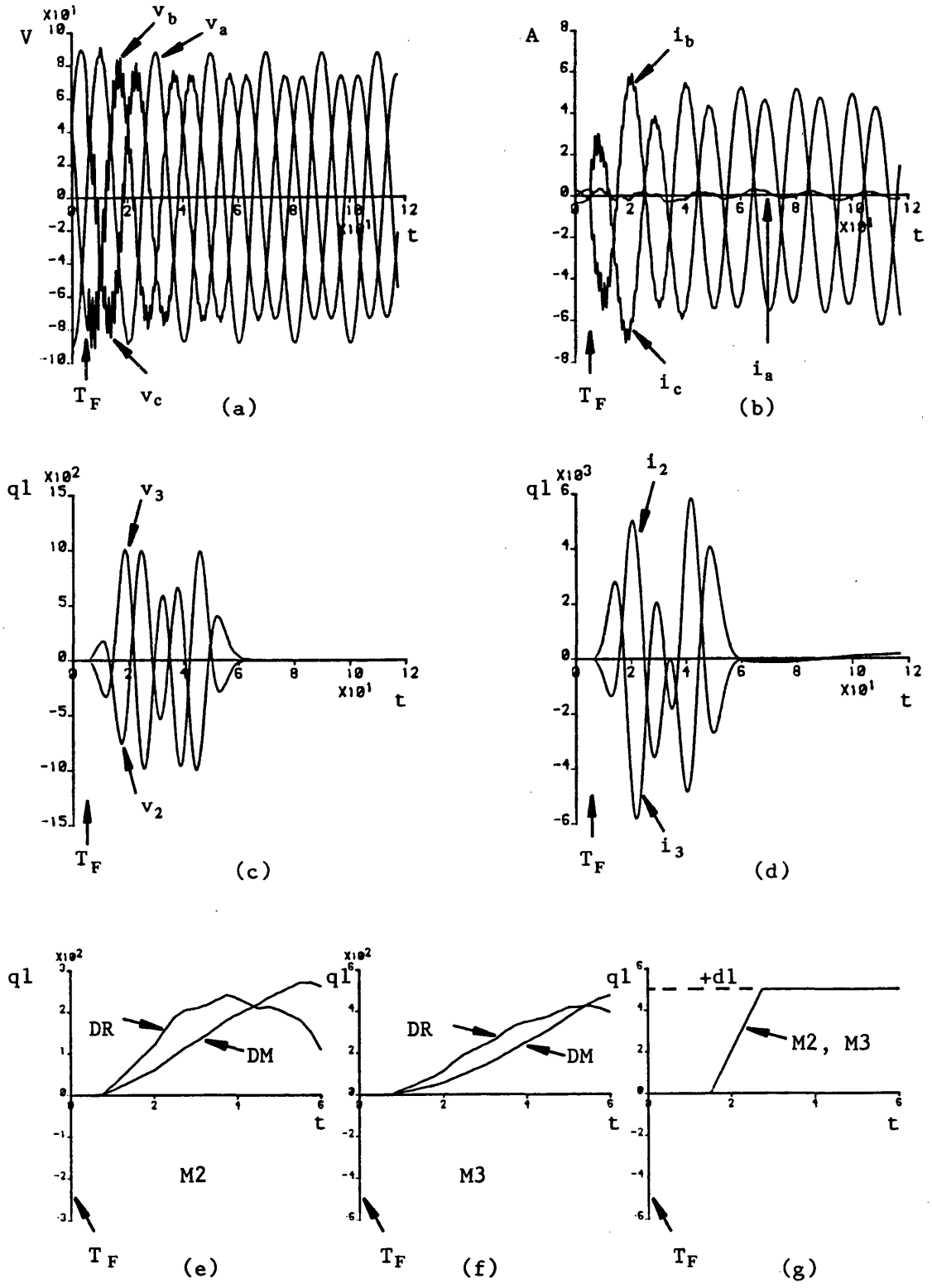


Fig 7.12 Waveforms at various stages within relay at P for 'b' to 'c' to earth fault

(a) and (b) Pre-filtered input voltages and currents

(c) and (d) Filtered superimposed modal voltages and currents

(e) and (f) M2 and M3 detailed, DM and DR responses

(g) Trip counter outputs

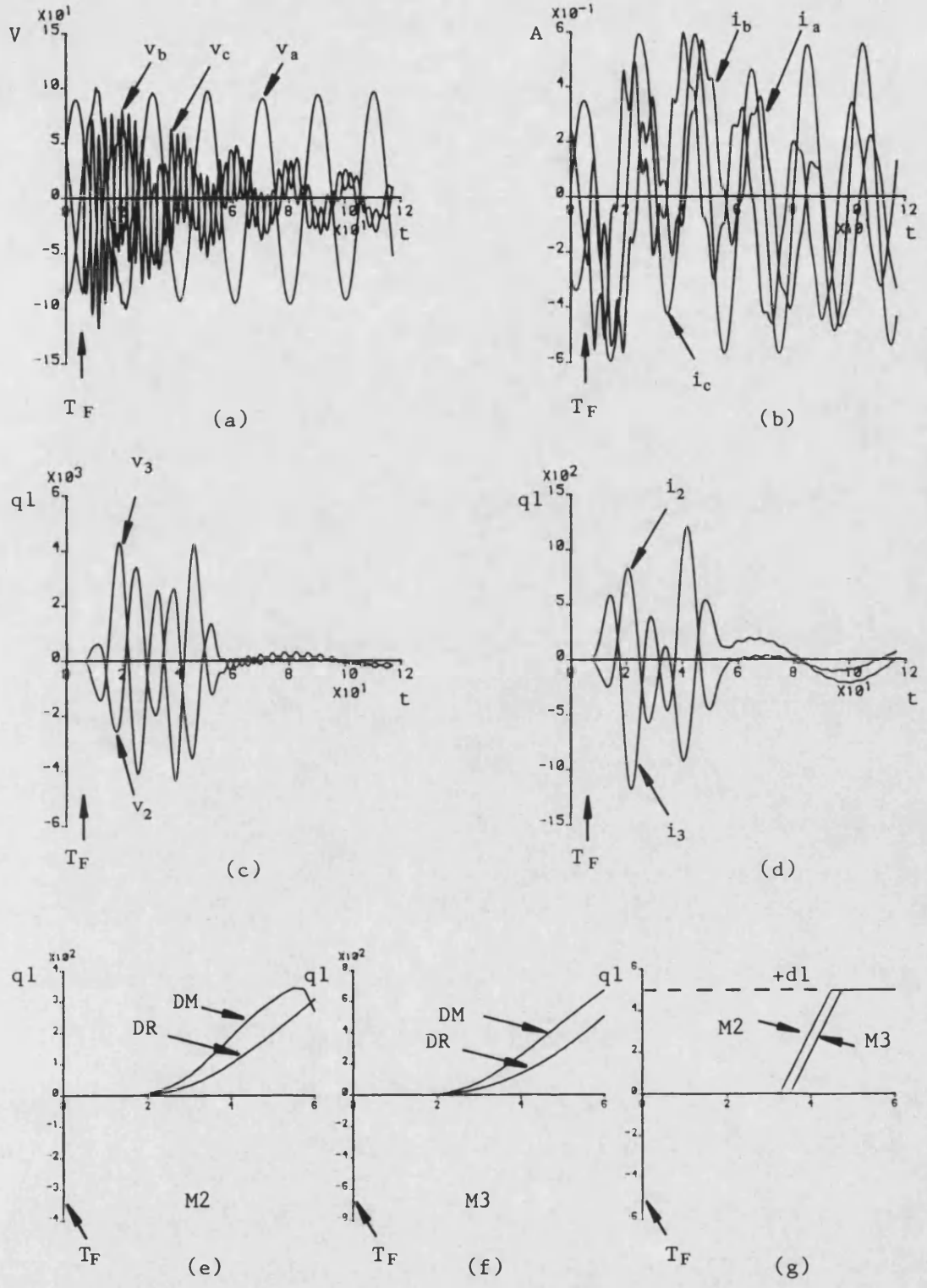


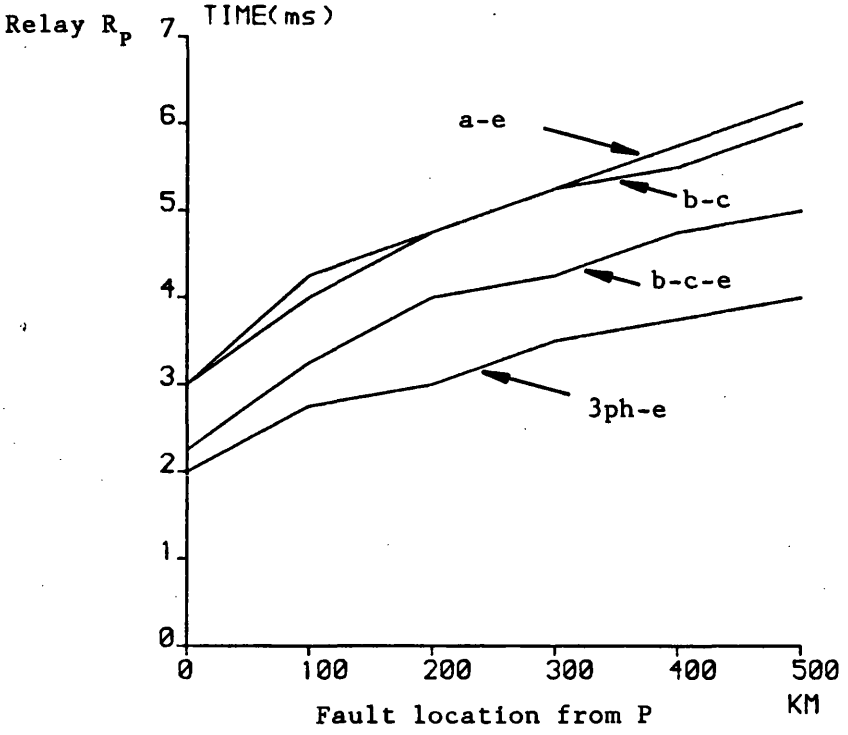
Fig 7.13 Waveforms at various stages within relay at Q for 'b' to 'c' to earth fault

(a) and (b) Pre-filtered input voltages and currents

(c) and (d) Filtered superimposed modal voltages and currents

(e) and (f) M2 and M3 detailed, DM and DR responses

(g) Trip counter outputs



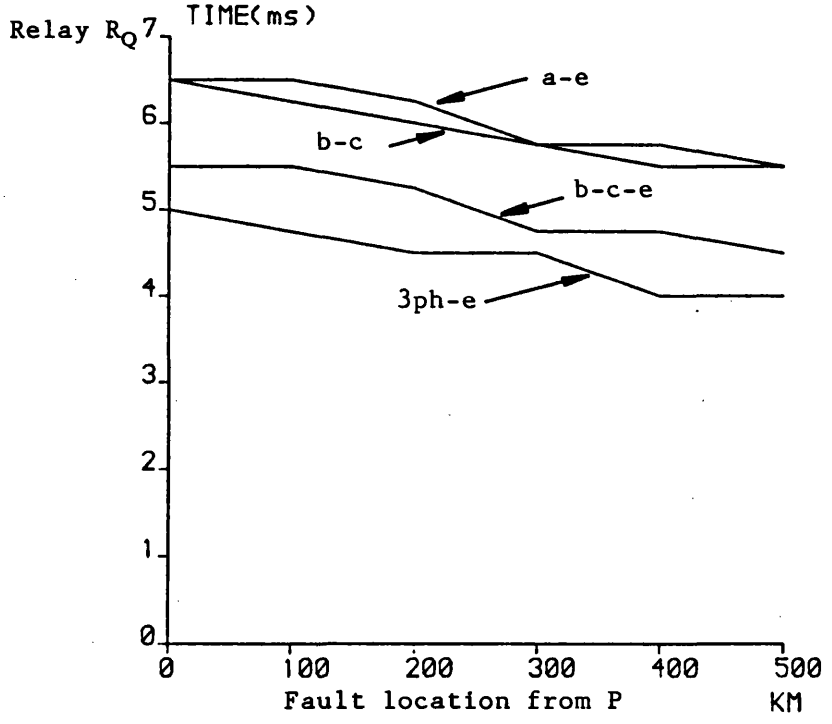
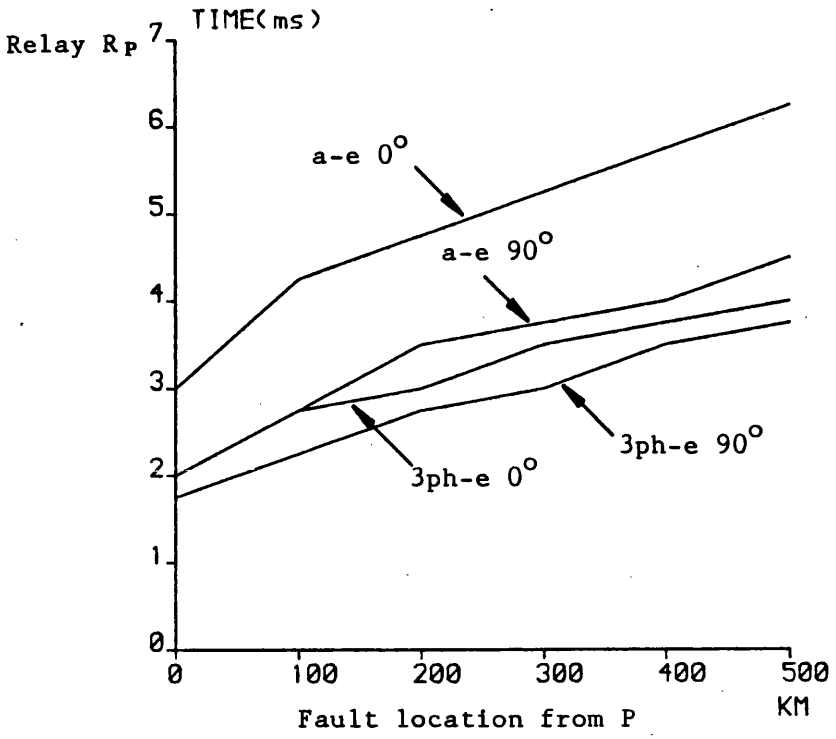


Fig 7.14 Fault Type/Fault Location characteristics for relays R_P and R_Q



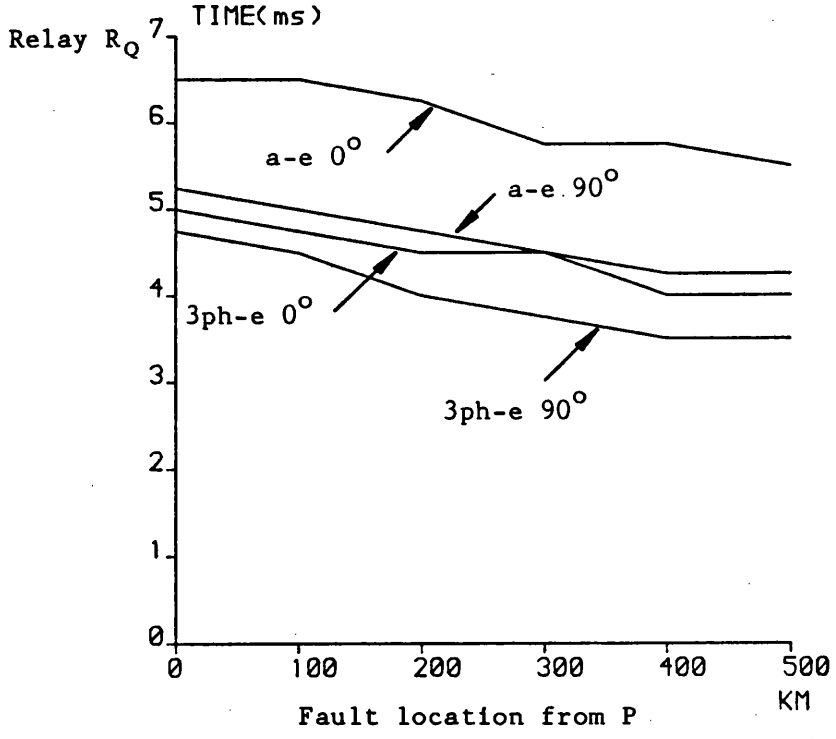
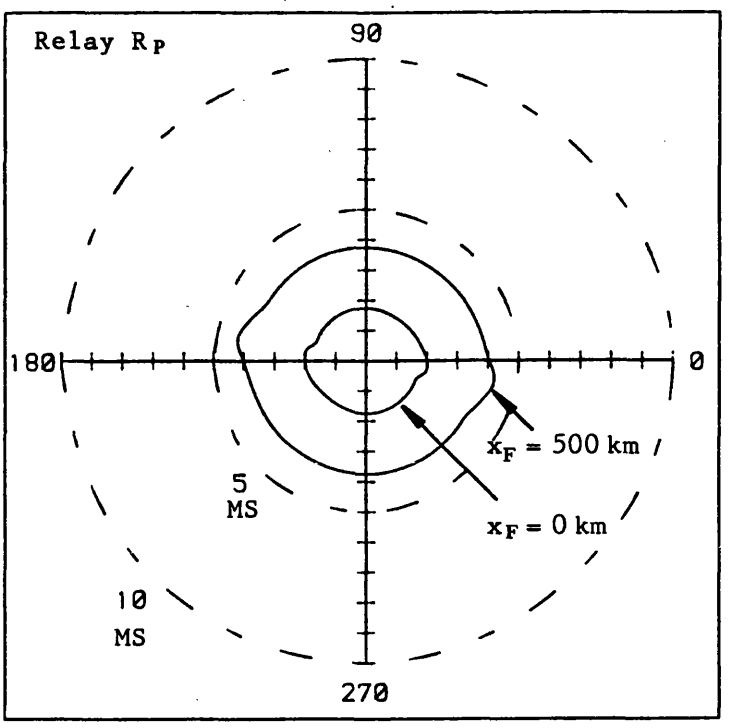


Fig 7.15 Fault inception angle/fault location characteristics for relays R_P and R_Q, fia referred to 'a' phase



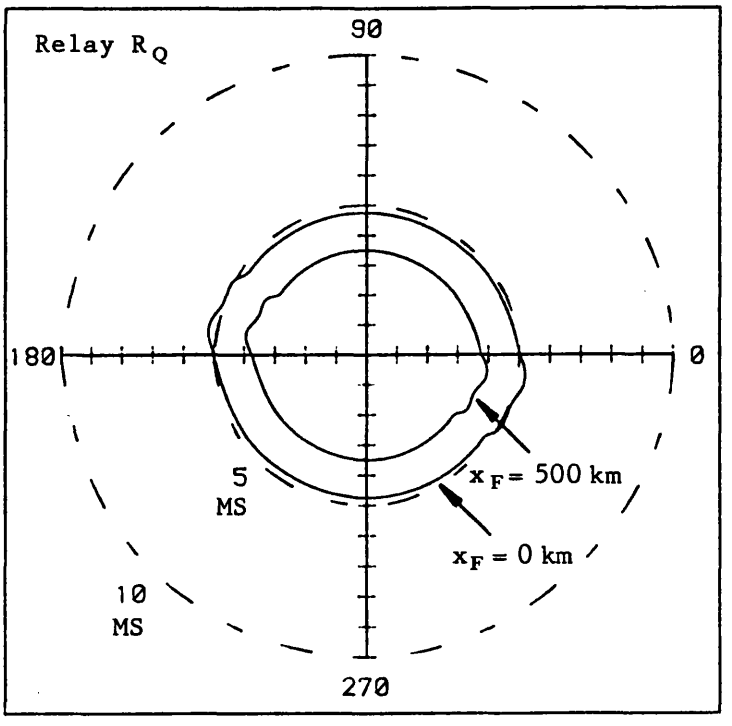
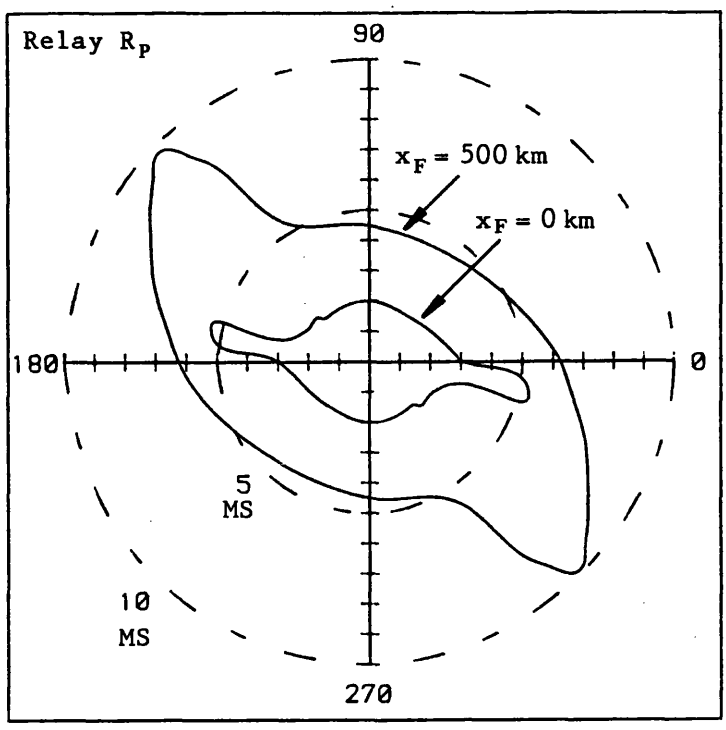


Fig 7.16 Polar fault inception angle/operating time characteristics for 3 phase to earth faults and fault location $x_F = 0$ and 500 km from end P



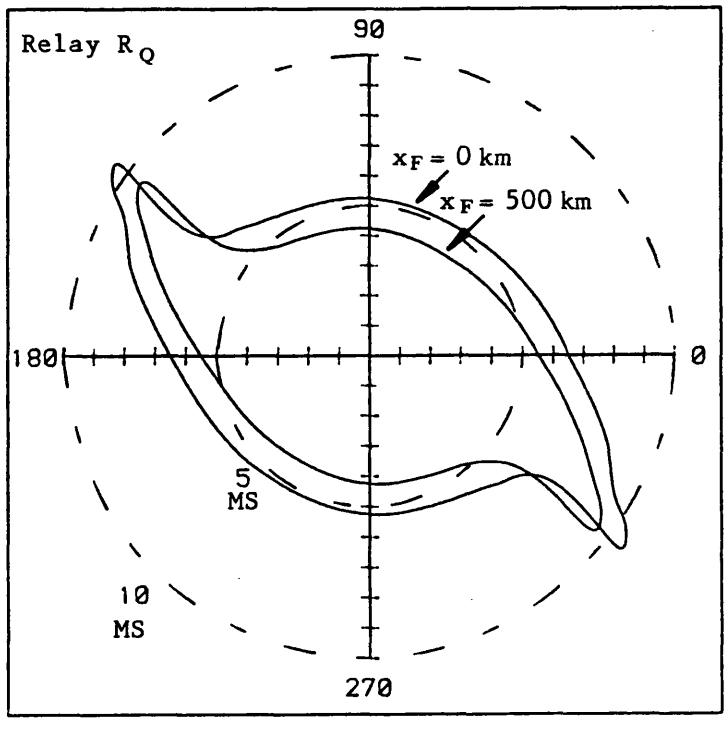


Fig 7.17 Polar fault inception angle/operating time characteristics for 'a' to earth faults and fault location $x_F = 0$ and 500 km from end P

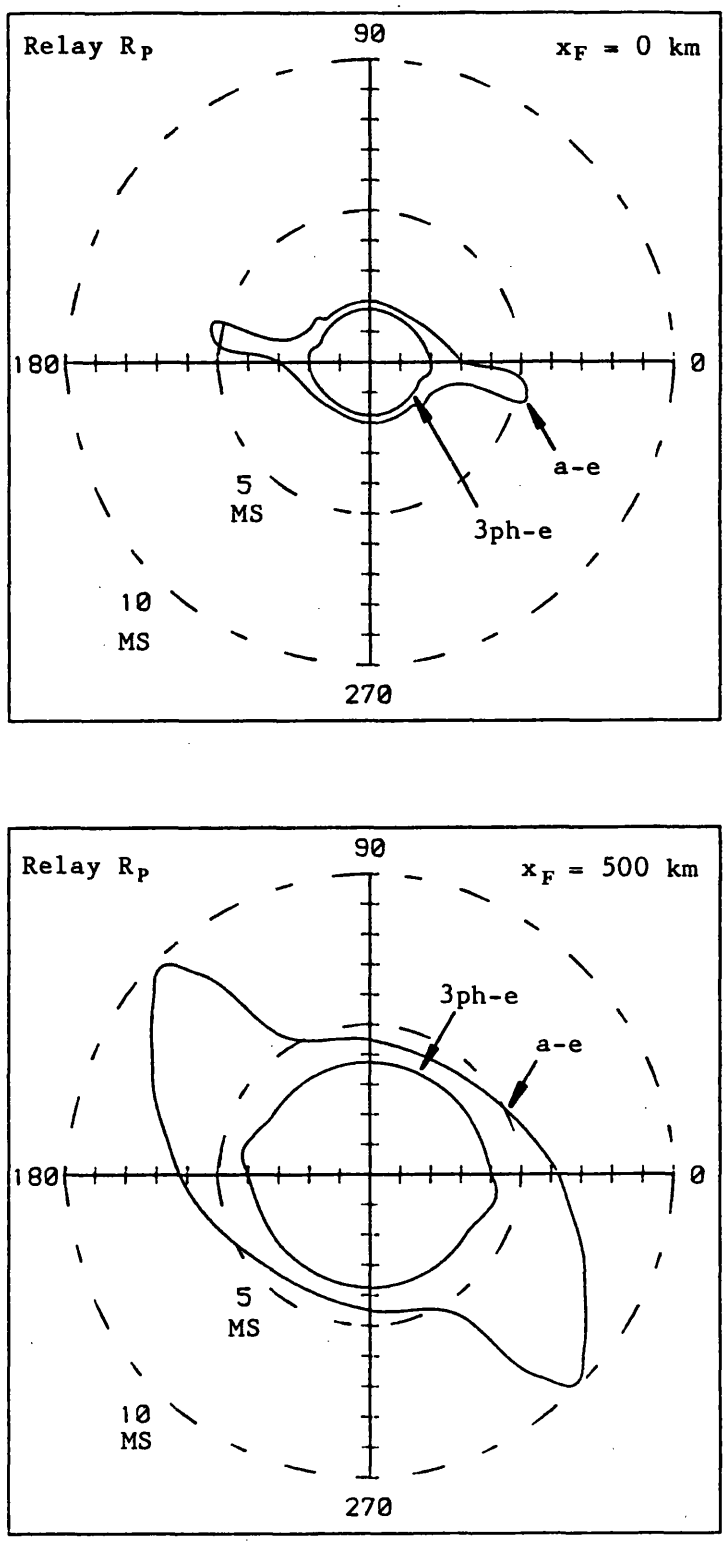
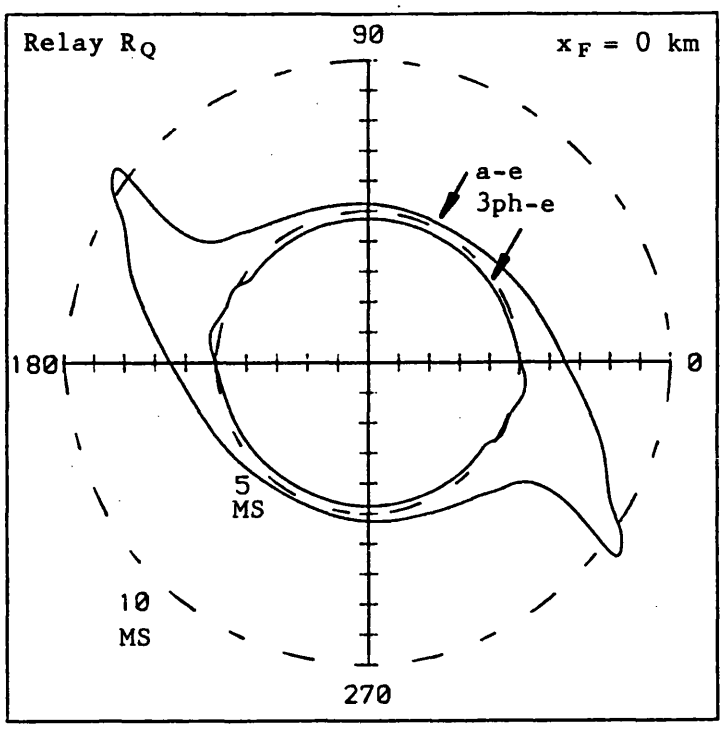


Fig 7.18 Polar comparison characteristics for relay R_P of fault inception angle/operating time with 3 phase and single phase to earth faults, x_F = 0 and 500 km from end P



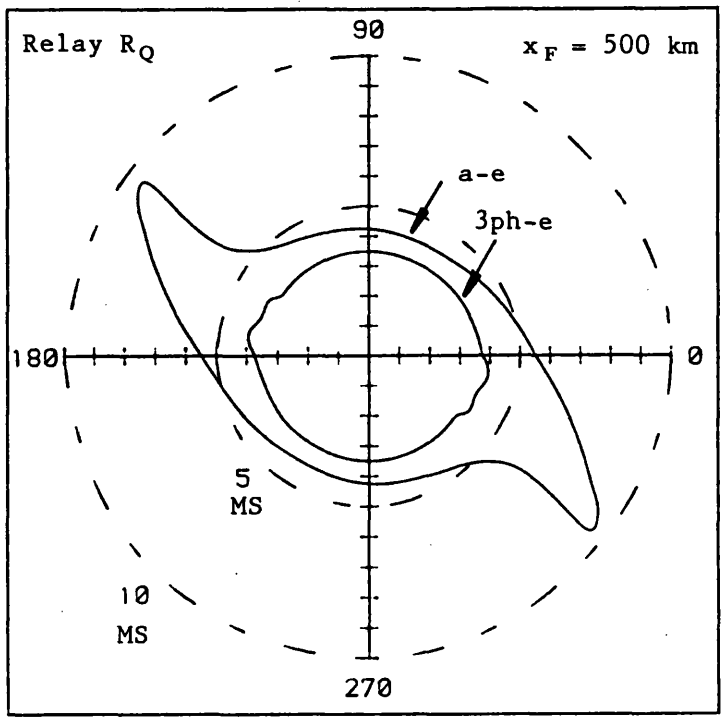


Fig 7.19 Polar comparison characteristics for relay R_Q of fault inception angle/operating time with 3 phase and single phase to earth faults, x_F = 0 and 500 km from end P

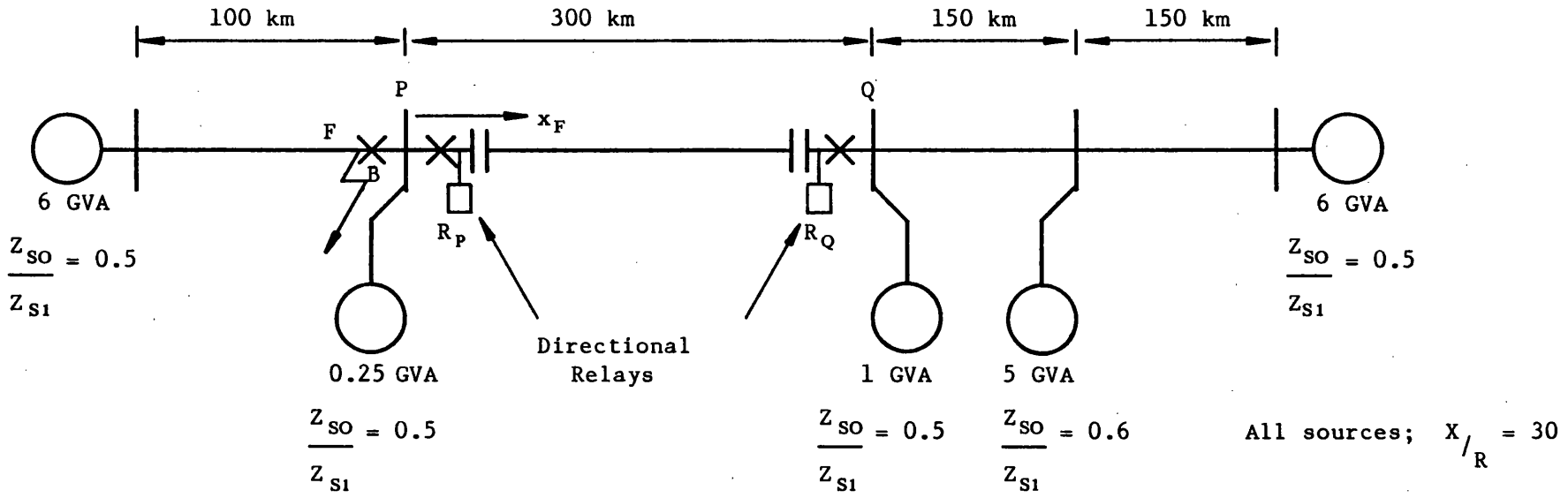
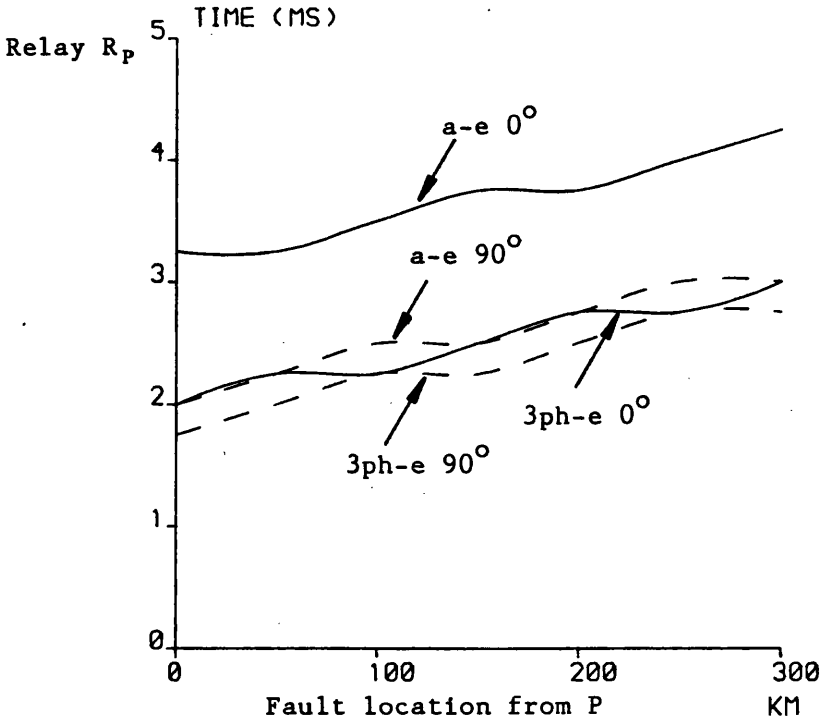


Fig 7.20 Multi-section feeder, with series compensated main line P-Q, with directional relays at ends P and Q



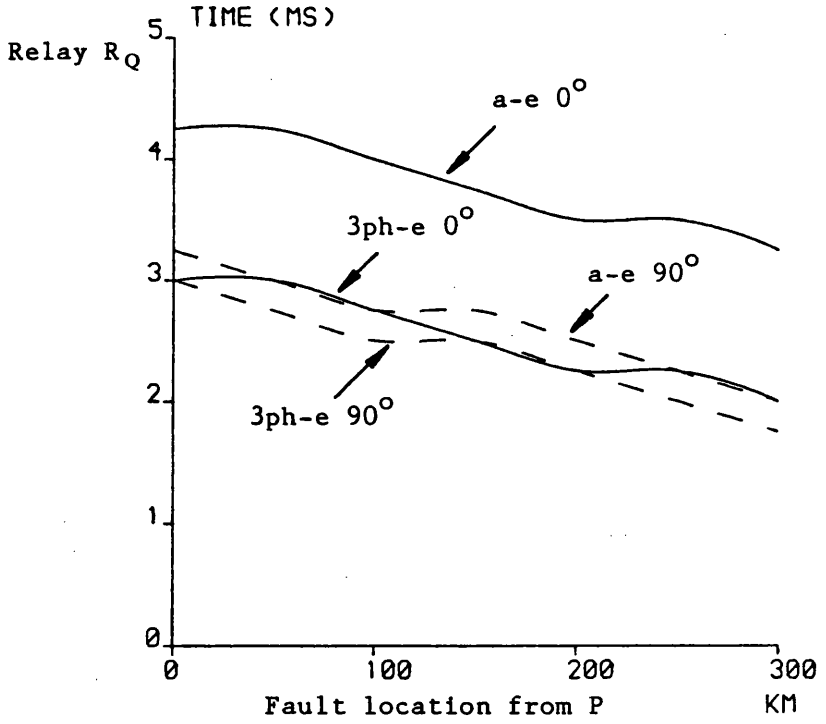
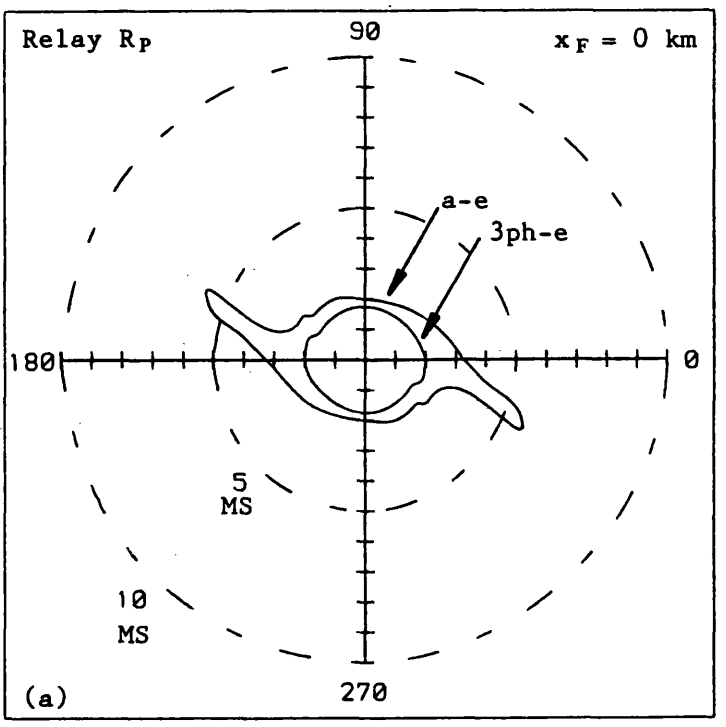


Fig 7.21 Fault inception angle/fault location characteristics for relays R_P and R_Q on typical system of Fig 7.20, fia referred to 'a' phase



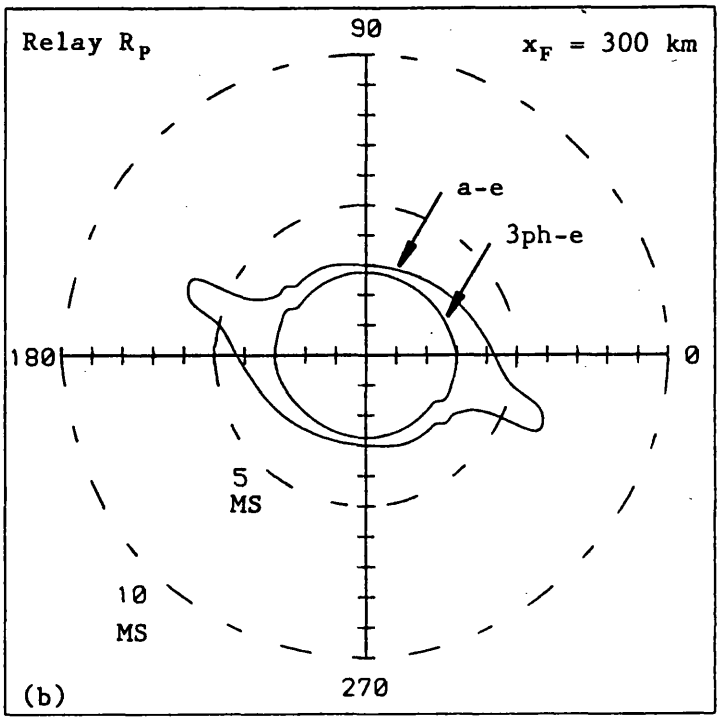
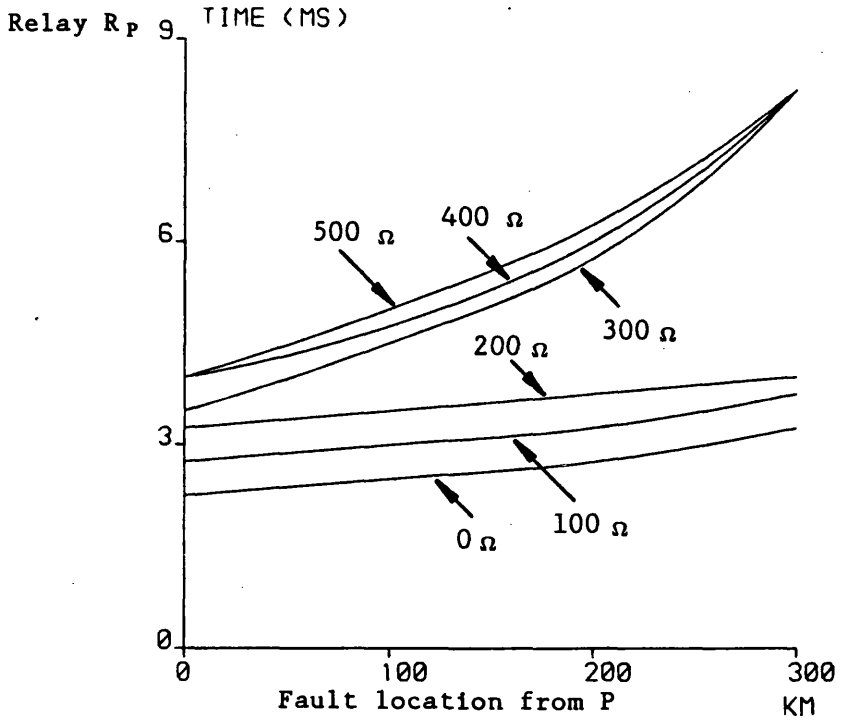


Fig 7.22 Polar comparison characteristics for relay R_P of fault inception angle/operating time for system of Fig 7.20, x_F = 0 and 300 km from end P



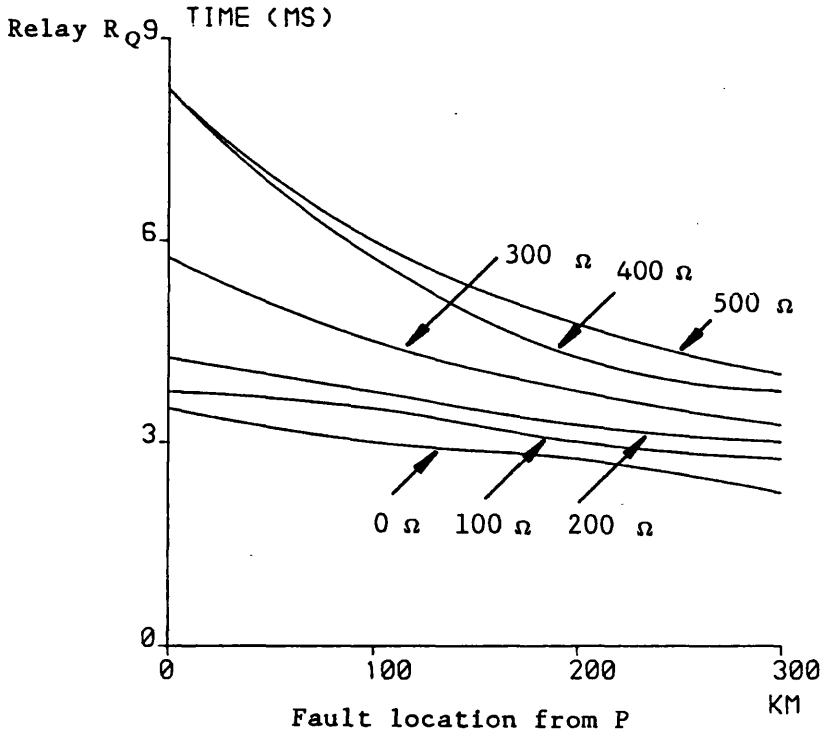


Fig 7.23 Fault path resistance/operating time characteristics for system of Fig 7.20, x_F = 0 to 300 km from end P, R_F = 0 to 500 Ω

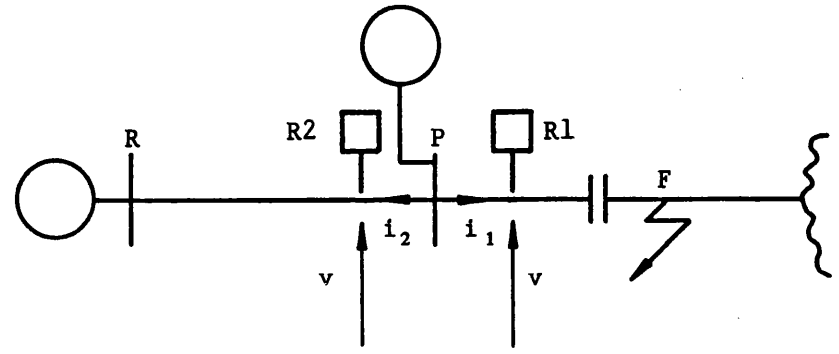


Fig 7.24 Faulted section of Fig 7.20 (circuit breakers omitted) for capacitive fault current study

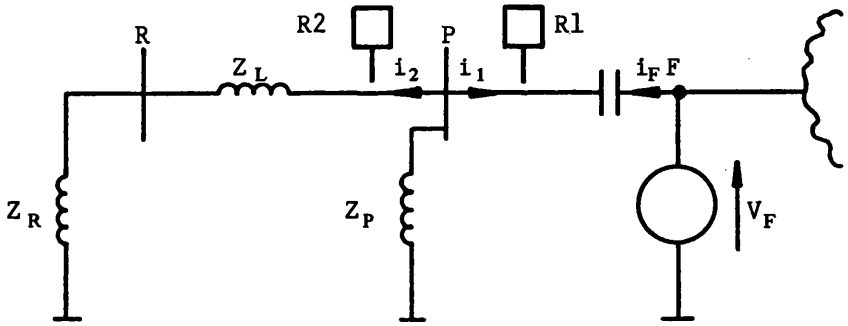


Fig 7.25 De-energised fault transient model for Fig 7.24

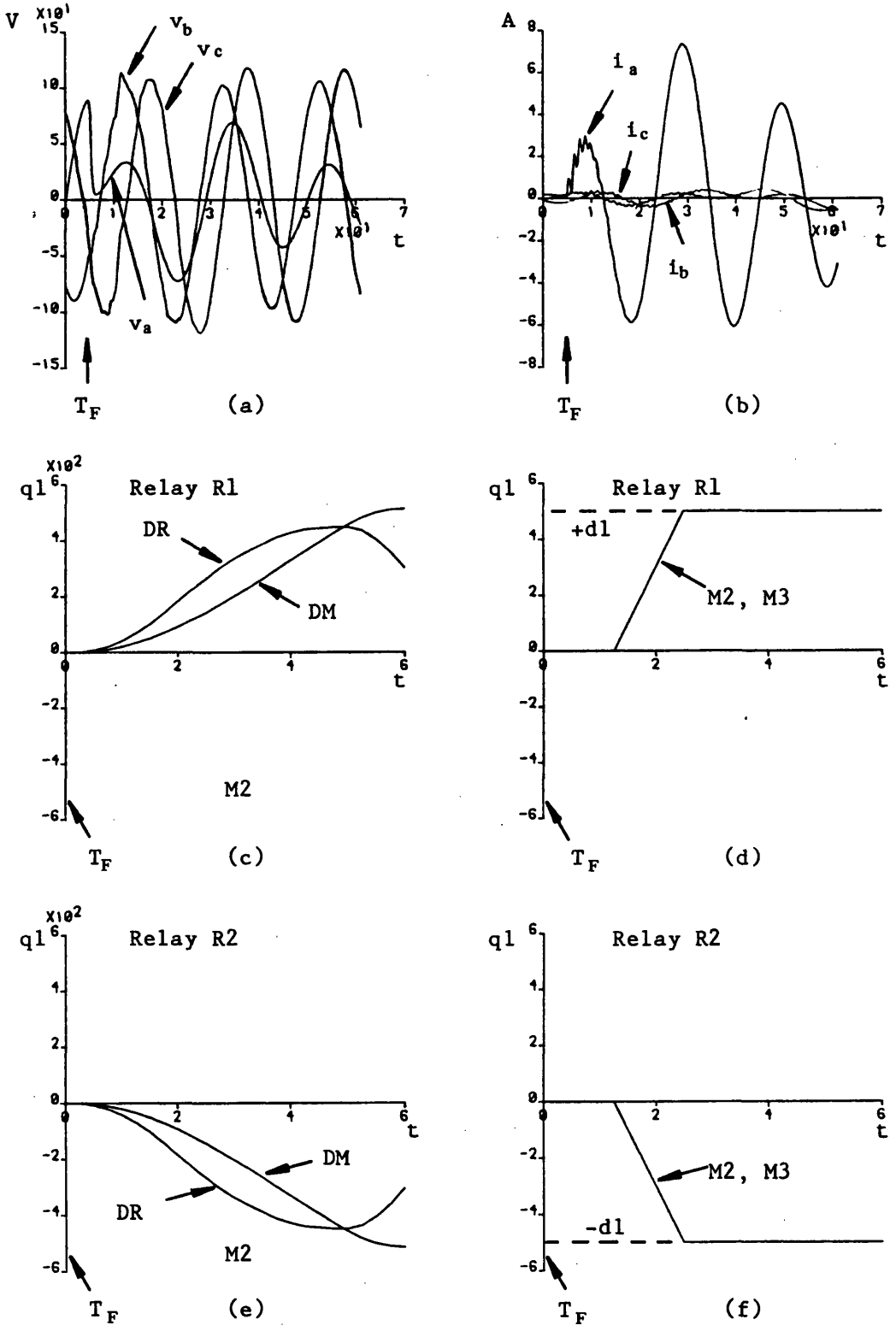
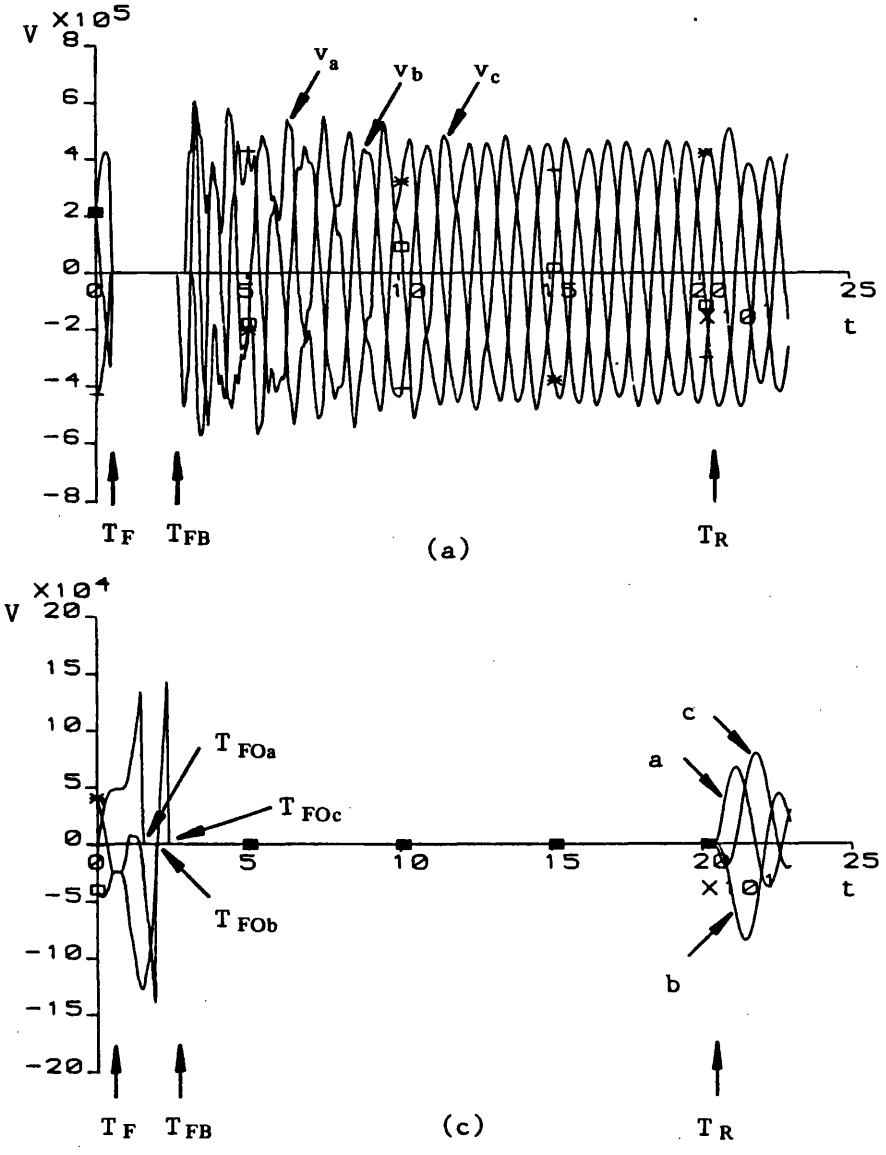


Fig 7.26 Responses of relays R1 and R2 to 'a'-'e' fault at F (Fig 7.24)



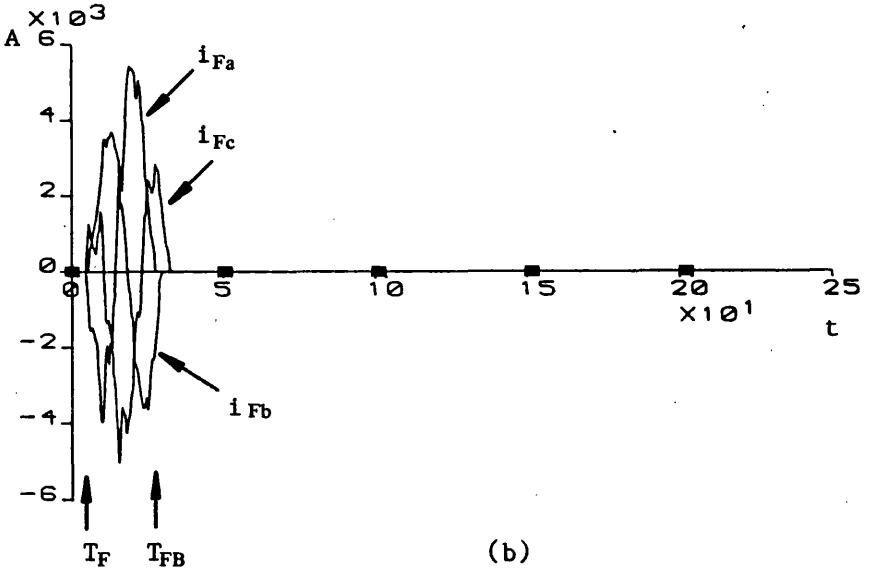


Fig 7.27 Primary system waveforms for 3 phase to earth external fault, with capacitor reinsertion

(a) Phase voltages at busbar P

(b) Line currents (equivalent fault path currents) flowing through circuit breaker B

(c) End P capacitor voltages, simultaneously reinserted at time t = T_R, 200 ms post fault

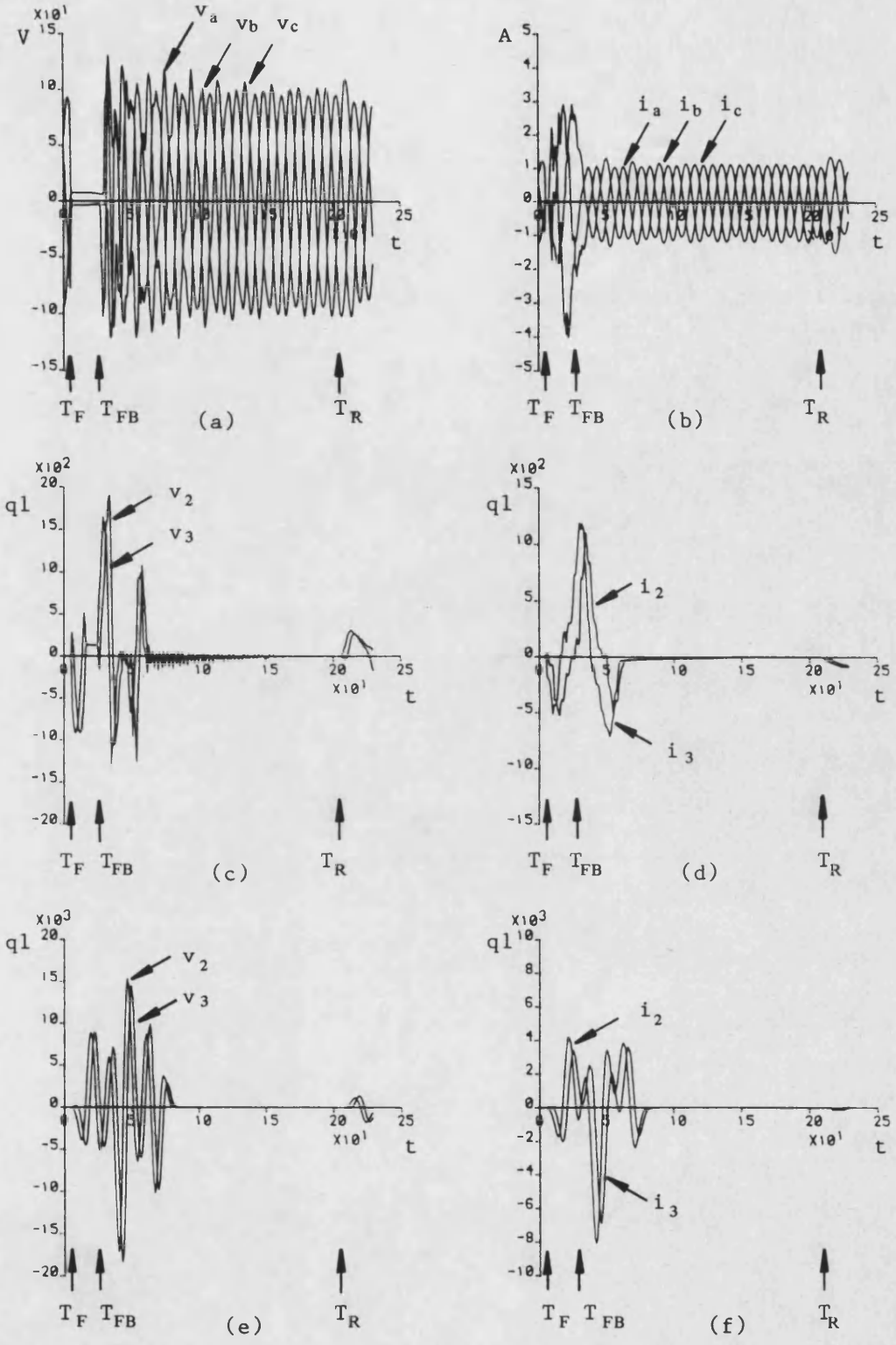
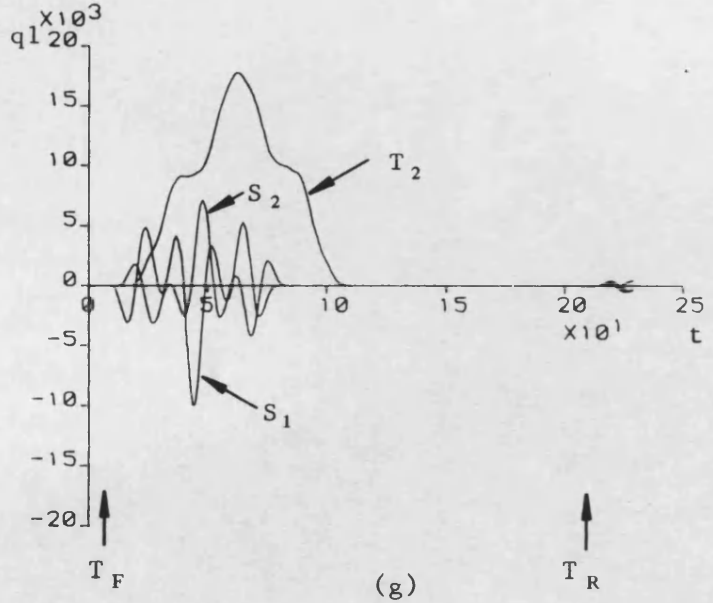


Fig 7.28 Signal variations within relay R_P, for 3 phase to earth external fault

(a) and (b) Pre-filtered input voltages and currents

(c) and (d) Superimposed M2 and M3 voltages and currents

(e) and (f) Filtered forms of (c) and (d)



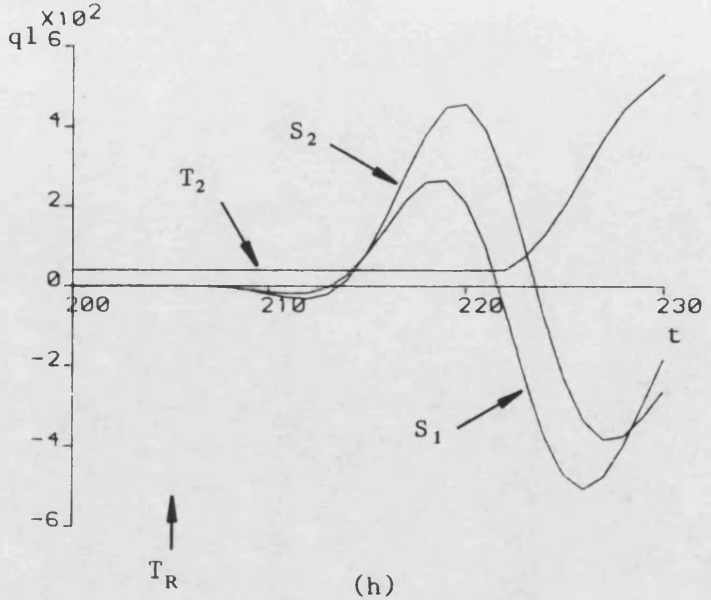
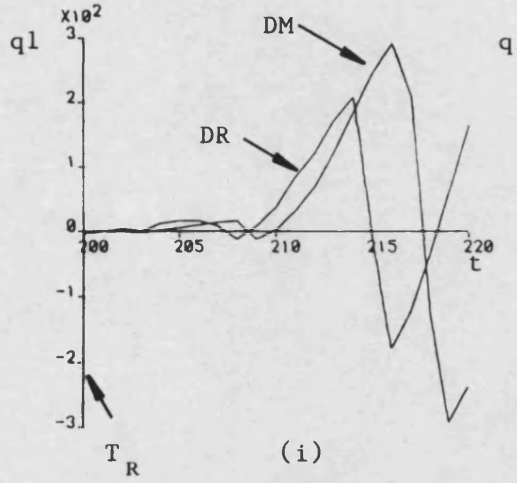
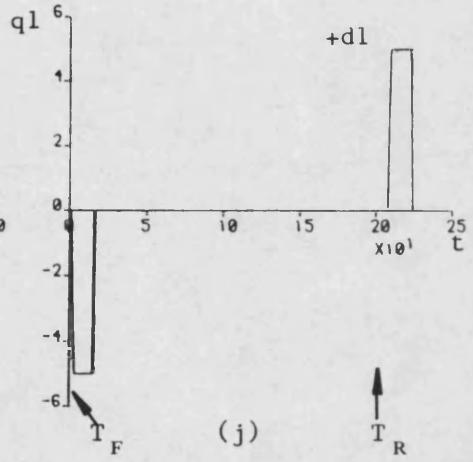


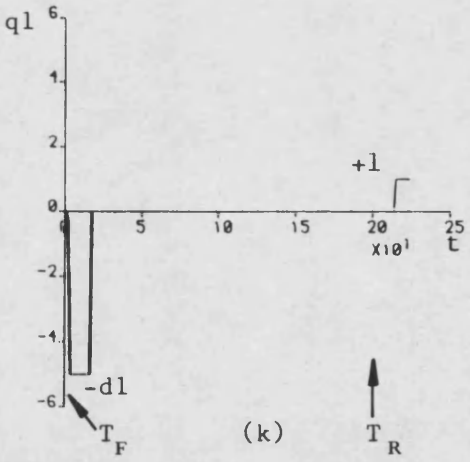
Fig 7.28 cont'd

(g) M2 relaying signal variations

(h) Detailed M2 relaying signal variations







(i) Detialed M2 DM and DR responses

(j) Trip counter output (M2) showing -dl for fault detection and +dl for reinsertion

(k) Trip counter output (M2) with increased T_2 minimum level

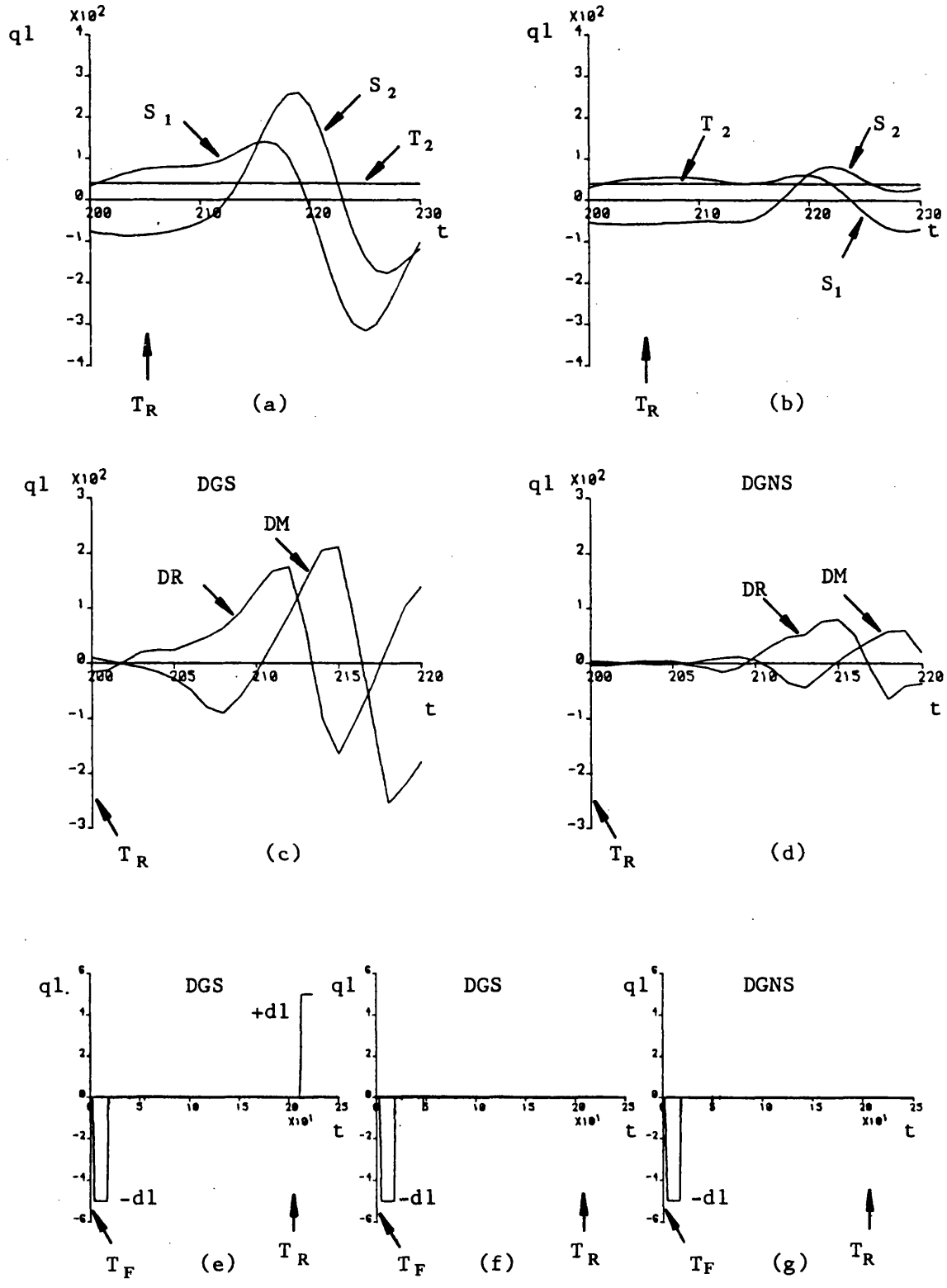


Fig 7.29 Signal variations within relay R_P, for a single phase to earth external fault, obtained with DGS and DGNS capacitor protection

(a) and (b) Detailed M2 relaying signal variations

(c) and (d) Detialed M2 DM and DR responses

(e) M2 Trip counter, DGS, T_{2MIN} = 40 ql

(f) M2 Trip counter, DGS, T_{2MIN} = 65 ql

(g) M2 Trip counter, DGNS, T_{2MIN} = 40 ql

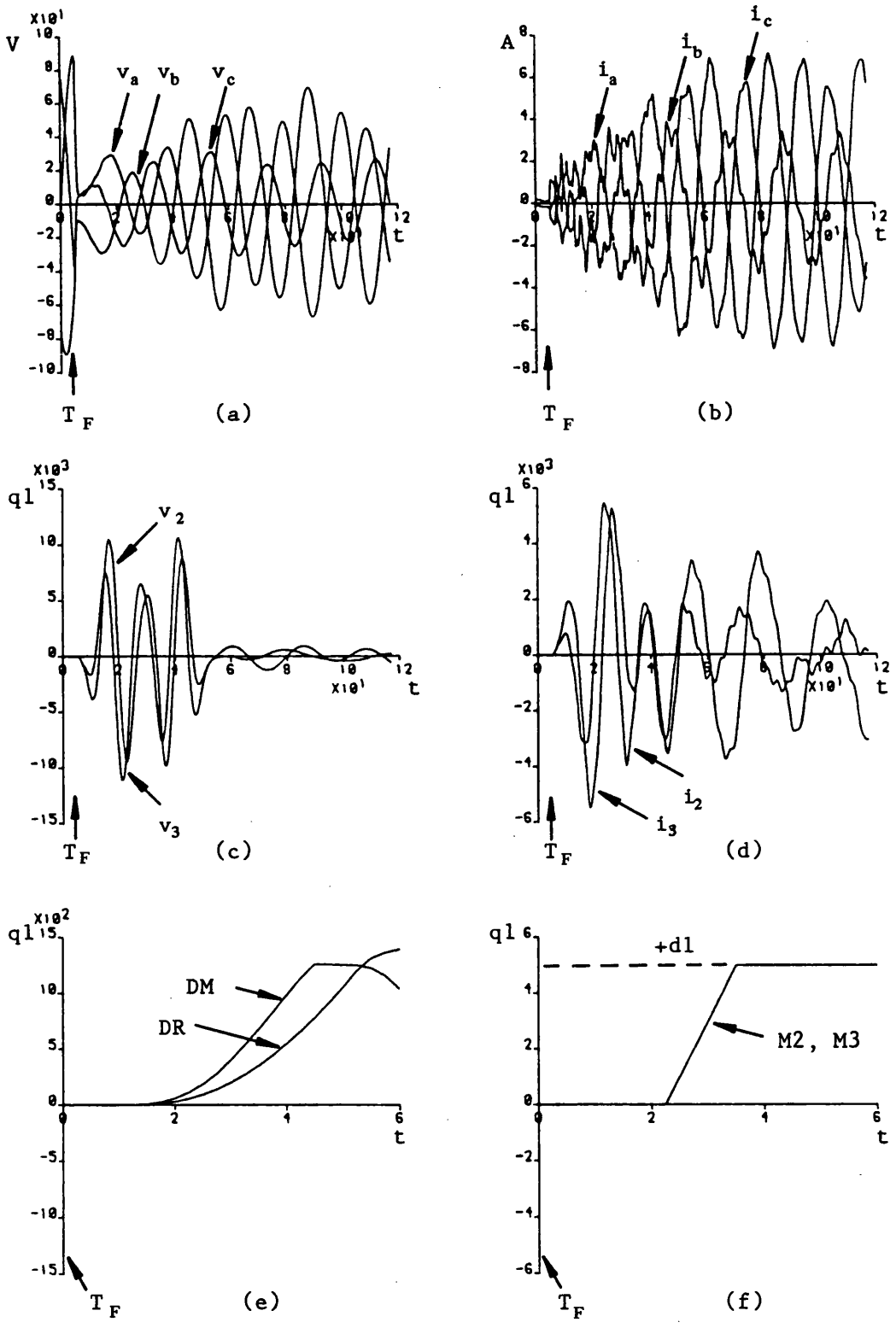


Fig 7.30 Waveforms within relay R1 for remote 3 phase to earth fault on double circuit system of Fig 7.2a

(a) and (b) Prefiltered input voltages and currents

(c) and (d) M2 and M3 filtered, superimposed voltages and currents

(e) Detailed M2 DM and DR response

(f) Trip counter outputs

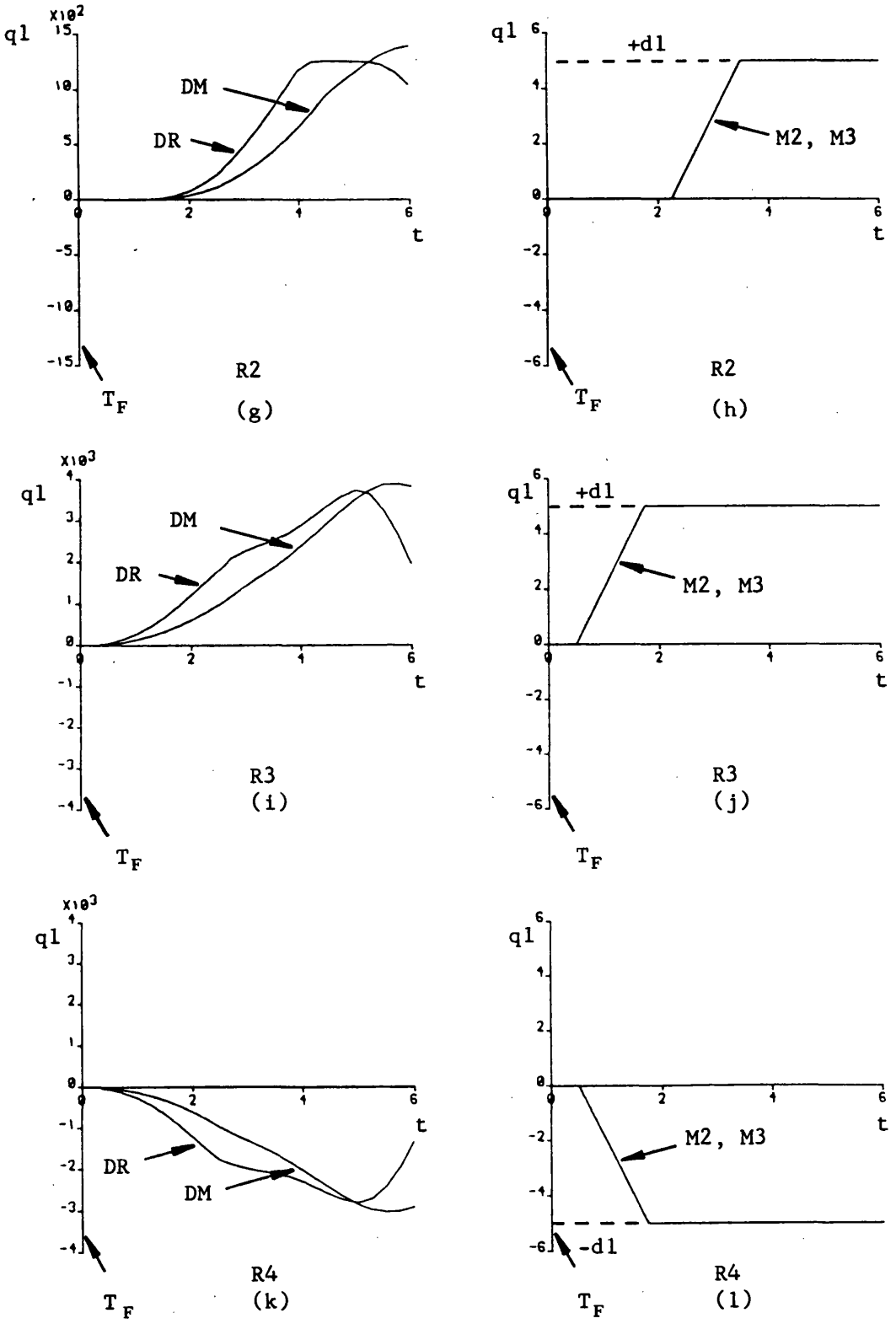


Fig 7.30 cont'd

(g) Detailed M2 DM and DR responses at R2

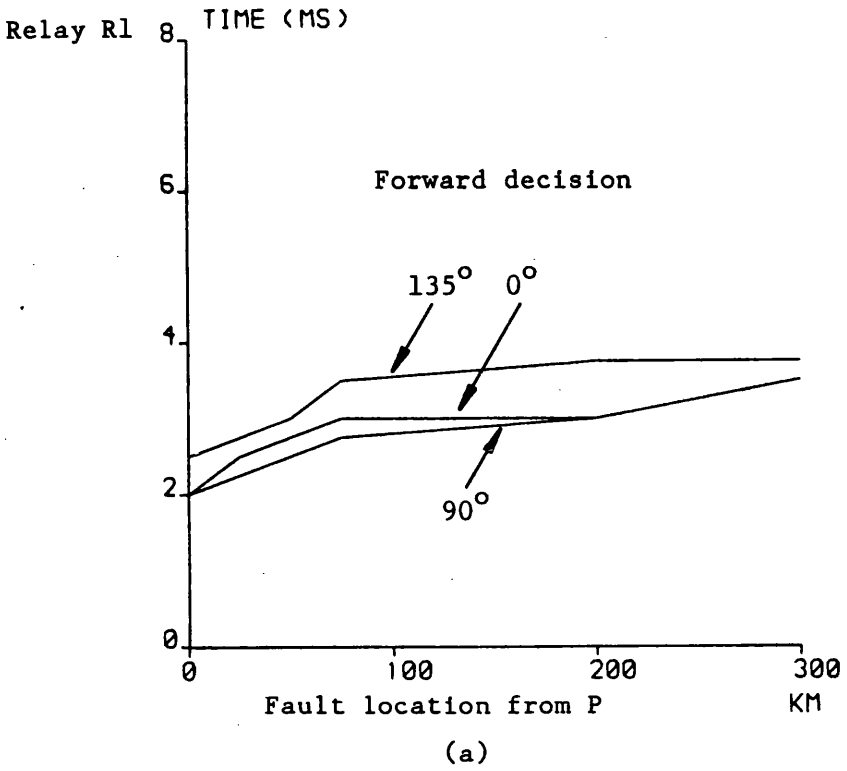
(h) Trip counter outputs of R2 (Fwd decision)

(i) Detailed M2 DM and DR responses at R3

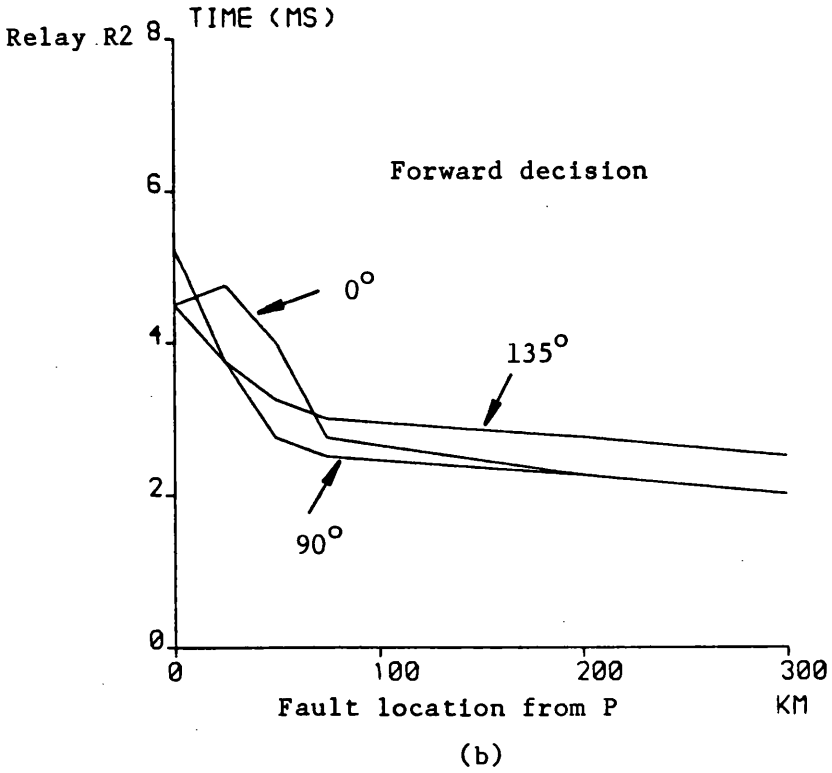
(j) Trip counter outputs of R3 (Fwd decision)

(k) Detailed M2 DM and DR responses at R4

(l) Trip counter outputs of R4 (Rev decision)

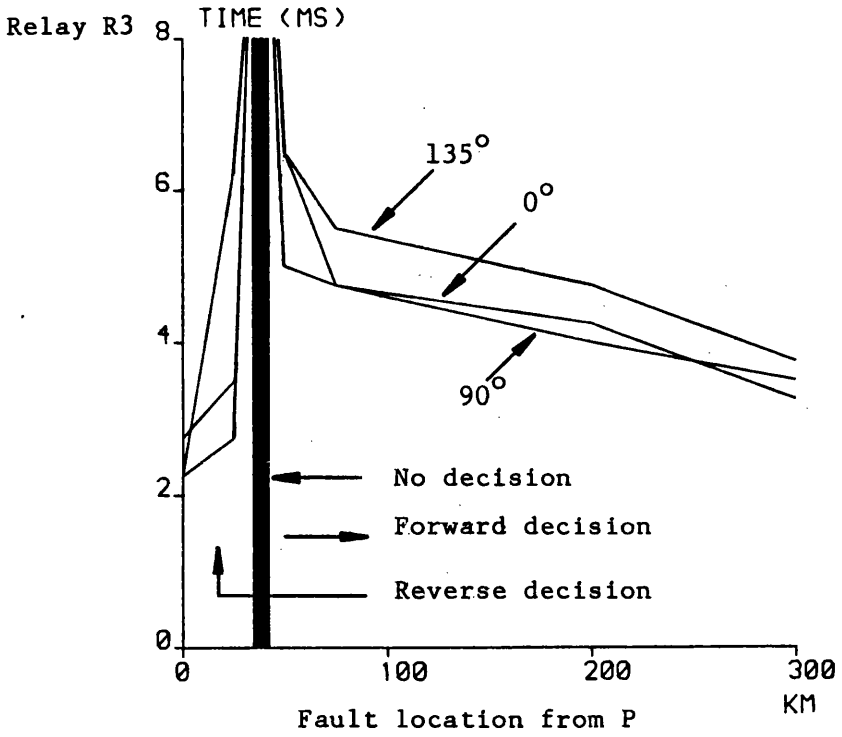


(a)



(b)

Fig 7.31 Fault angle/fault location/operating time characteristics for solid 'b' phase to earth faults on circuit 1 of double circuit system of Fig 7.2a, responses of relays Rl and R2



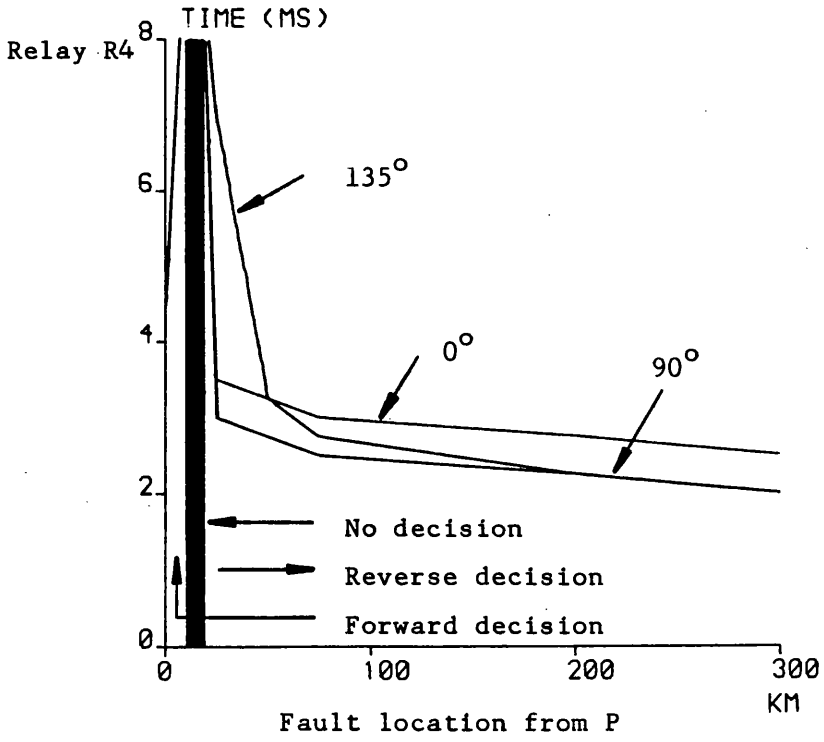


Fig 7.32 Response of relays R3 and R4 for fault conditions as in Fig 7.29, describing the change in directional indications by the healthy circuit relays

CHAPTER 8: CONCLUSIONS AND FUTURE WORK

8.1 General Conclusions

The work presented in this thesis describes the design and performance of a new directional comparison protection scheme, as applied to series compensated systems. Based upon new principles, it is not simply a travelling wave relay, but a relay which utilises the total superimposed components impressed upon the system steady state variations, in order to render high speed directional decisions. Not being an impedance measuring device, nor employing segregated phase signal processing, the relay has proven to offer reliable operation under the following conditions;

a) Internal or external faults, regardless of type.

b) With or without any line loading.

c) With or without series capacitor by-passing.

d) Resonant conditions at subsynchronous frequencies.

e) High fault path resistances.

For both single and double circuit systems, the longstanding protection problems associated with conventional protection, and in particular, distance relays, have been dealt with in some detail. In all situations, the proposed relay performs exceptionally well, for all practically encountered faults with the overall performance of the relay as a function of fault inception angle, distance to fault, fault type, etc, being quite outstanding. The problems concerning capacitor by-passing and subsequent reinsertion are overcome by

optimisation of the relay settings. For external faults in particular, not causing capacitor by-passing, and giving rise to subsynchronous resonant conditions, it has been demonstrated how the specially developed dynamic threshold function serves to stabilise the relay, ie to prevent any mal-operation, subsequent to an initial reverse decision.

The fault transient data used for evaluating the relay performance has been obtained using digital simulation techniques which have been validated using recently performed field tests. In the case of single circuit systems, the simulation methods have been extended to include the most recent versions of independent capacitor protection equipment. The absence of capacitor by-passing facilities for the double circuit simulations has not in any way detracted from the performance evaluation of the relay, as most line protection problems encountered with such systems are brought about by the capacitors remaining in circuit for the fault duration.

The subtle combinaton of time and frequency domain simulation techniques have enabled the accurate modelling of the state of the art in capacitor protection, that is the Dual Gap/Non-Linear resistor scheme. The methodology involved is fully explained and contributes a major step forward in the simulation of series compensated systems and to their understanding. Results have shown that the proposed relay will operate correctly for any type of capacitor protection whether the latter is called upon to operate for a particular fault condition or not. It is for the situation where capacitor reinsertion into an energised system takes place that the above mentioned simulation techniques have revealed that the Dual

Gap/Non-Linear Resistor scheme provides benefits not only from a system stability point of view, but also with respect to line relaying.

The directional wave fault detection principles have been extended from fundamental directional theory, based upon information superimposed onto the prefault variations, due to the occurrence of a fault. The underlying principles have proven valid and the specialised filtering techniques developed to enhance the security of decision whilst retaining high speed operating capability have been explained. Such was the filtering and monitoring philosophy adopted that the presence of subsynchronous resonance, known to be problematical for phase comparison and distance relays, in no way jeopardises the initial relay response and the latter has been fully stabilised until such time as the subsynchronous components die out.

With the superimposed component extraction and signal processing being performed digitally, considerable improvements over analogue equivalents, have been made. These include freedom from drift, reduced noise and delay, since at the instant of the change in relaying point voltage and current, due to the occurrence of a fault, the superimposed components are immediately available at the outputs of the extraction stages (excluding digital propagation delays).

Moreover, the software programming of the digital filter characteristics can be executed at the outset for a particular system application, with no possibility of ambient temperature or age distorting the filter characteristics.

Since the relaying signals are formed from Aerial mode superimposed quantities alone, significant advantages over the segregated three phase approach have been achieved. These include:

a) Reduction in signal processing requirements from six separate channels to four.

b) Analysis of circuit behaviour under faulted conditions is achieved using the familiar phase sequence equivalent circuits, this being of particular interest to an experienced application engineer being confronted with new relaying principles. Moreover, the first application dependent gain to be set is derived from simple pps equivalent circuits alone.

c) High speed coverage of all fault types with only two sets of modal relaying signals, with reliable relay operation even when only one mode is excited.

d) Independent relaying of each circuit in double circuit applications, provided the two separate Aerial mode paths do not interfere with one another, ie that faults on one circuit do not develop into intercircuit faults.

The use of superimposed components for detecting faults has yielded benefits in terms of high sensitivity in particular for highly

resistive fault paths. This feature is particularly important in very dry countries where faults involve a line section and vegetation, or where the earth plane is particularly resistive.

One other major benefit of superimposed component based relays is the rapid detection of close-up three phase solid faults which have the greatest de-stabilising effect upon the system. Distance protection requires additional memory circuitry to counteract the total collapse of all three line to earth voltages, whereas, the superimposed signals are infact the largest that can be obtained for a fault anywhere on the system, resulting in very high speed fault detection with no special modifications to the relaying algorithm. Moreover, superimposed components offer inherent gains in signal to noise ratio with instrument transformers. The well known cvt relaxation transients do not detract significantly from the superimposed signals from which the relay makes a decision.

The expected form of hardware implementation of the new relay developed from CAD studies, is directly compatable with present and future generations of 16 bit microprocessors. Such quantisation yields a dynamic relaying signal range which is more than adequate for the relay to derive sufficient fault transient information to render a correct directional decision, for the vast number of fault conditions which may arise. Moreover, with the perpetual refinement of LSI and VLSI devices, coupled with improvements in device reliability, it is expected that such designs will become the norm in years hence.

8.2 Suggestions for Future Work

Although the specific problem encountered with conventional relays of series capacitors being located on infeeding lines, behind the relaying point, has been analysed by an equivalent fault condition in which capacitor by-passing does not occur, the inclusion of series capacitors on infeeding lines in the digital system simulation would be beneficial. This is so because over very long distances, such as in the USA, a number of line sections, each of which are series compensated, are often linked together. Many double circuit systems are configured in this way and the further extension for the simulations to facilitate capacitor by-passing for such systems would directly contribute to the realism of the simulations as a whole.

The non-linear analysis, developed as a combination of time and frequency domain techniques, to simulate the Dual Gap/Non-Linear resistor capacitor by-pass protection scheme, has in this thesis been limited to single phase operation. The author feels, despite single phase to earth faults being the most commonly occurring type on ehv systems, that extensions to the existing software to include multiphase capacitor by-passing, would be beneficial.

For the directional relaying scheme proposed, it is hoped that the computer algorithms will be implemented in hardware form and that subsequent field trials would ensue. This would enable the measurement of actual values of noise, generated both from the relay hardware and that from the primary system, discussed in Chapter 6. The setting procedure adopted could then be refined to include these practical noise levels, which may then prove more realistic than those assumed in the text.

APPENDIX A2.1: UNIVERSAL MATRIX FORMULATION

Considering the relationships between the end P variables and the fault point of Fig 2.4, the following two port relation is available;

$$\begin{bmatrix} \overline{E}_{PCk} \\ -\overline{I}_{PCk} \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} \overline{V}_{Pk} \\ -\overline{I}_{Pk} \end{bmatrix} \qquad \text{--- A2.1.1}$$

and $\overline{V}_{Pk} = -Z_P . \overline{I}_{Pk}$

therefore $\overline{E}_{PCk} = -A_1 . Z_P . \overline{I}_{Pk} - B_1 . \overline{I}_{Pk}$
$= -(A_1 . Z_P + B_1) . \overline{I}_{Pk}$

and $\overline{I}_{PCk} = (C_1 . Z_P + D_1) . \overline{I}_{Pk}$

hence $\underline{\overline{E}_{PCk} = Z_A . \overline{I}_{PCk}}$ --- A2.1.2

where $Z_A = -(A_1 . Z_P + B_1) . (C_1 . Z_P + D_1)^{-1}$

At the capacitor bank, it is convenient to relate all variables to the forcing quantity $\overline{E}_{CPk}$ as follows;

$$\overline{I}_{PCk} = \overline{I}_{CPk} + Z_C^{-1} . \overline{E}_{DPk}$$

but $\overline{E}_{DPk} = \overline{E}_{CPk} + Z_{D2} . \overline{I}_{CPk}$

hence $\overline{I}_{PCk} = \overline{I}_{CPk} + Z_C^{-1} (\overline{E}_{CPk} + Z_{D2} . \overline{I}_{CPk})$

and $\overline{I}_{PCk} = \overline{I}_{CPk} . [U + Z_C^{-1} . Z_{D2}] + Z_C^{-1} . \overline{E}_{CPk}$

or $\underline{\overline{I}_{PCk} = K_1 . \overline{I}_{CPk} + Z_C^{-1} . \overline{E}_{CPk}}$ --- A2.1.3

where $K_1 = [U + Z_C^{-1} . Z_{D2}]$

Now $\overline{V}_{PCk} = \overline{E}_{PCk} - \overline{E}_{DPk}$

$= Z_A . \overline{I}_{PCk} - [\overline{E}_{CPk} + Z_{D2} . \overline{I}_{CPk}]$

$= Z_A . [K_1 . \overline{I}_{CPk} + Z_C^{-1} . \overline{E}_{CPk}] - [\overline{E}_{CPk} + Z_{D2} . \overline{I}_{CPk}]$

$= [Z_A . K_1 - Z_{D2}] . \overline{I}_{CPk} + [Z_A . Z_C^{-1} - U] . \overline{E}_{CPk}$

or $\underline{\overline{V}_{PCk} = Z_B . \overline{I}_{CPk} + K_2 . \overline{E}_{CPk}}$ --- A2.1.4

where $Z_B = [Z_A . K_1 - Z_{D2}]$ and $K_2 = [Z_A . Z_C^{-1} - U]$

The second line section yields the following two port relation;

$$\begin{bmatrix} \overline{V}_{Fk} \\ -\overline{I}_{FPk} \end{bmatrix} = \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} \overline{V}_{PCk} \\ -\overline{I}_{PCk} \end{bmatrix}$$

thus $\overline{V}_{Fk} = A_2.\overline{V}_{PCk} - B_2.\overline{I}_{PCk}$

and $\overline{I}_{FPk} = -C_2.\overline{V}_{PCk} + D_2.\overline{I}_{PCk}$

Substituting for $\overline{V}_{PCk}$ in Eq A2.1.4;

$$\overline{V}_{Fk} = A_2.[Z_B.\overline{I}_{CPk} + K_2.\overline{E}_{CPk}] - B_2.[K_1.\overline{I}_{CPk} + Z_C^{-1}.\overline{E}_{CPk}]$$

or $\overline{V}_{Fk} = [A_2.Z_B - B_2.K_1].\overline{I}_{CPk} + [A_2.K_2 - B_2.Z_C^{-1}].\overline{E}_{CPk}$

ie $$\underline{\overline{V}_{Fk} = Z_D.\overline{I}_{CPk} + K_3.\overline{E}_{CPk}} \qquad \text{--- A2.1.5}$$

where $Z_D = [A_2.Z_B - B_2.K_1]$ and $K_3 = [A_2.K_2 - B_2.Z_C^{-1}]$

similarly;

$$\underline{\overline{I}_{FPk} = K_4.\overline{I}_{CPk} + Y_A.\overline{E}_{CPk}} \qquad \text{--- A2.1.6}$$

where $K_4 = [D_2.K_1 - C_2.Z_B]$ and $Y_A = [D_2.Z_C^{-1} - C_2.K_2]$

from Eq A2.1.6

$$\overline{I}_{CPk} = K_4^{-1}.\overline{I}_{FPk} + K_4^{-1}.Y_A.\overline{E}_{CPk}$$

and substituting this into Eq A2.1.5 gives;

$$\overline{V}_{Fk} = Z_D.K_4^{-1}.\overline{I}_{FPk} + [Z_D.K_4^{-1}.Y_A + K_3].\overline{E}_{CPk}$$

or $$\underline{\overline{V}_{Fk} = Z_D.K_4^{-1}.\overline{I}_{FPk} + K_5.\overline{E}_{CPk}} \qquad \text{--- A2.1.7}$$

where $K_5 = [Z_D\, K_4^{-1} Y_A + K_3]$

The fault point voltage $\overline{V}_{Fk}$ may be related in a similar manner to the variables at end Q, which gives;

$$\underline{\overline{V}_{Fk} = Z_Q.K_7^{-1}.\overline{I}_{FQk} + K_8.\overline{E}_{CQk}} \qquad \text{--- A2.1.8}$$

Where Z_Q, K_7 and K_8 are functions of the end Q source parameters and the line section ABCD parameters between F and Q. Now from Eqs A2.1.7 and A2.1.8.

$$\bar{I}_{FPk} = K_4 . Z_D^{-1} . \bar{V}_{Fk} - K_4 . Z_D^{-1} . K_5 . \bar{E}_{CPk}$$

and $$\bar{I}_{FQk} = K_7 . Z_G^{-1} . \bar{V}_{Fk} - K_7 . Z_G^{-1} . K_8 . \bar{E}_{CQk}$$

but $$\bar{I}_{Fk} = \bar{I}_{FPk} - \bar{I}_{FQk} \text{ and } \bar{V}_{Fk} = \bar{E}_{Fk} + R_F . \bar{I}_{Fk}$$

hence $$I_{Fk} = [K_4 . Z_D^{-1} - K_7 . Z_G^{-1}] . \bar{V}_{Fk} - K_4 . Z_D^{-1} . K_5 . \bar{E}_{CPk} - K_7 . Z_G^{-1} . K_8 . \bar{E}_{CQk}$$

So $$\bar{I}_{Fk} = Y_C . [\bar{E}_{Fk} + R_F . \bar{I}_{Fk}] - K_4 . Z_D^{-1} . K_5 . \bar{E}_{CPk} - K_7 . Z_G^{-1} . K_8 . \bar{E}_{CQk}$$

$$= Y_C . \bar{E}_{Fk} + Y_C . R_F . \bar{I}_{Fk} - K_4 . Z_D^{-1} . K_5 . \bar{E}_{CPk} - K_7 . Z_G^{-1} . K_8 . \bar{E}_{CQk}$$

where $$Y_C = [K_4 . Z_D^{-1} - K_7 Z_G^{-1}]$$

then $$\bar{I}_{Fk} = [K_{10} . Y_C] . \bar{E}_{Fk} - [K_{10} . K_4 . Z_D^{-1} . K_5] . \bar{E}_{CPk} - [K_{10} . K_7 . Z_G^{-1} . K_8] . \bar{E}_{CQk} \qquad \text{--- A2.1.9}$$

where $$K_{10} = [U - Y_C . R_F]^{-1}$$

Eq A2.1.9 is in the form;

$$\bar{I}_{Fk} = Y_1 . \bar{E}_{Fk} + Y_2 . \bar{E}_{CPk} + Y_3 . \bar{E}_{CQk}$$

and this then forms the first row of a universal admittance relation;

$$\begin{bmatrix} \bar{I}_{Fk} \\ \bar{I}_{CPk} \\ \bar{I}_{CQk} \end{bmatrix} = \begin{bmatrix} Y_1 & Y_2 & Y_3 \\ Y_4 & Y_5 & Y_6 \\ Y_7 & Y_8 & Y_9 \end{bmatrix} \begin{bmatrix} \bar{E}_{Fk} \\ \bar{E}_{CPk} \\ \bar{E}_{CQk} \end{bmatrix} \qquad \text{--- A2.1.20}$$

The other sub-matrices Y_4, ... Y_9 are determined from Eqs A2.1.1 to A2.1.9 in a similar manner.

Eq A2.1.10 is then inverted to produce the universal impedance relation in the form of Eq 2.6, but depending upon the type of disturbance being simulated, it is often more convenient to utilise the admittance matrix of Eq A2.1.10.

APPENDIX A2.2: THEVIN EQUIVALENT CALCULATIONS

Looking from point P into the faulted section R-P, the equivalent impedance is found from Fig 2.8 by setting $\overline{E}_F$ to zero. The Thevenin impedance is then defined as the ratio of $\overline{E}_{FE}$ to $\overline{I}_{FE}$ or in vector terms $Z_{FE} = \overline{E}_{FE} \cdot \overline{I}_{FE}^{-1}$. At this stage it is worth mentioning that the fault point situation is best represented by a parallel admittance matrix, Y_F, to ground. This is because of phase to phase fault conditions which give rise to ill-conditioning when series representation R_F is inverted.

Thevenin Impedance

For calculation of the impedance term Z_{FE}, it is necessary to determine equivalent admittances of the system. From the fault point towards end R, the following two port relation is available;

$$\begin{bmatrix} \overline{V}_F \\ -\overline{I}_{FR} \end{bmatrix} = \begin{bmatrix} A_{RF} & B_{RF} \\ C_{RF} & D_{RF} \end{bmatrix} \begin{bmatrix} U & Z_R \\ 0 & U \end{bmatrix} \begin{bmatrix} 0 \\ \overline{I}_R \end{bmatrix} \qquad \text{--- A2.2.1}$$

from which;

$$\overline{V}_F = (A_{RF} \cdot Z_R + B_{RF}) \cdot \overline{I}_R \qquad \text{--- A2.2.2}$$

and $$\overline{I}_{FR} = (C_{RF} \cdot Z_R + D_{RF}) \cdot \overline{I}_R \qquad \text{--- A2.2.3}$$

then $$\underline{\overline{I}_{FR} = Y_2 \cdot \overline{V}_F} \qquad \text{--- A2.2.4}$$

where $$Y_2 = (C_{RF} \cdot Z_R + D_{RF})(A_{RF} \cdot Z_R + B_{RF})^{-1}$$

hence $$Y_2 = \overline{I}_{FR} \cdot \overline{V}_F^{-1} \qquad \text{--- A2.2.5}$$

Y_2 Represents the admittance presented to the fault point looking towards end R. Hence an equivalent circuit is drawn as in Fig A 2.2.1 ($\overline{E}_F$ set to zero), from which the addition of the two admittances Y_2 and Y_F is inverted to give an equivalent impedance term, Z_E such that;

$$Z_E = (Y_2 + Y_F)^{-1} \qquad \text{--- A2.2.6}$$

Then the equivalent circuit of Fig A2.2.2 is used to relate $\overline{E}_{FE}$ and $\overline{I}_{FE}$ as follows;

$$\begin{bmatrix} \overline{E}_{FE} \\ \overline{I}_{FE} \end{bmatrix} = \begin{bmatrix} A_{FP} & B_{FP} \\ C_{FP} & D_{FP} \end{bmatrix} \begin{bmatrix} U & Z_E \\ 0 & U \end{bmatrix} \begin{bmatrix} 0 \\ \overline{I}_E \end{bmatrix} \qquad \text{--- A2.2.7}$$

hence $\overline{E}_{FE} = (A_{FP}.Z_E + B_{FP})\overline{I}_E$ --- A2.2.8

and $\overline{I}_{FE} = (C_{FP}.Z_E + D_{FP})\overline{I}_E$ --- A2.2.9

then $\overline{E}_{FE} = (A_{FP}.Z_E + B_{FP})(C_{FP}.Z_E + D_{FP})^{-1}\overline{I}_{FE}$ --- A2.2.10

From Eq A2.2.10 the effective fault path impedance matrix Z_{FE} is simply;

$$\underline{Z_{FE} = \overline{E}_{FE}.\overline{I}_{FE}^{-1} = (A_{FP}.Z_E + B_{FP})(C_{FP}.Z_E + D_{FP})^{-1}} \qquad \text{--- A2.2.11}$$

Thevenin Voltage

With reference to the equivalent circuit of Fig 2.8, the fault point relationship is;

$$\overline{V}_F = \overline{E}_F + R_F.\overline{I}_F \qquad \text{--- A2.2.12}$$

But from the foregoing Z_{FE} calculations, $\overline{I}_{FR} = Y_2.\overline{V}_F$ and $\overline{V}_F$ may also be related to $\overline{I}_{FP}$ as follows;

$$\begin{bmatrix} \overline{V}_F \\ -\overline{I}_{FP} \end{bmatrix} = \begin{bmatrix} A_{FP} & B_{FP} \\ C_{FP} & D_{FP} \end{bmatrix} \begin{bmatrix} \overline{E}_{FE} \\ -\overline{I}_{FE} \end{bmatrix} \qquad \text{--- A2.2.13}$$

However, the open circuit voltages are determined when $\overline{I}_{FE} = 0$, hence;

$$\overline{V}_F = A_{FP}.\overline{E}_{FE} \qquad \text{--- A2.2.14}$$

and $$\overline{I}_{FP} = -C_{FP}.\overline{E}_{FE} \qquad \text{--- A2.2.15}$$

thus $$\overline{I}_{FP} = -C_{FP}.A_{FP}^{-1}.\overline{V}_F \qquad \text{--- A2.2.16}$$

or $$\overline{I}_{FP} = Y_1.\overline{V}_F \qquad \text{--- A2.2.17}$$

Now $\overline{I}_F = \overline{I}_{FP} - \overline{I}_{FR}$ may then be written as;

$$\overline{I}_{FP} - \overline{I}_{FR} = (Y_1 - Y_2)\overline{V}_F \qquad \text{--- A2.2.18}$$

hence $$\overline{V}_F = (Y_1 - Y_2)^{-1}.\overline{I}_F \qquad \text{--- A2.2.19}$$

Replacing V_F in Eq A2.2.12 gives;

$$(Y_1 - Y_2)^{-1}.\overline{I}_F = \overline{E}_F + R_F.\overline{I}_F \qquad \text{--- A2.2.20}$$

so that $$\overline{E}_F = [(Y_1 - Y_2)^{-1} - R_F)].\overline{I}_F \qquad \text{--- A2.2.21}$$

or $$\underline{\overline{E}_F = Z_{FF}.\overline{I}_F} \qquad \text{--- A2.2.22}$$

Equation A2.1.22 enables the calculation of $\overline{I}_F$ from any value of forcing quantity $\overline{E}_F$, which then yields the corresponding value of $\overline{V}_F$. The final step involves relating the fault point voltages $\overline{V}_F$ to the open circuit voltages $\overline{E}_{FE}$ near B, but such a relation has already been determined in Eq A2.2.14;

$$\overline{V}_F = A_{FP} \cdot \overline{E}_{FE}$$

hence $$\overline{E}_{FE} = A_{FP}^{-1} \cdot \overline{V}_F \qquad \text{--- A2.2.23}$$

By substituting for $\overline{V}_F$ in Eq A2.2.12;

$$\overline{E}_{FE} = A_{FP}^{-1}[\overline{E}_F + R_F \cdot \overline{I}_F]$$

or $$\underline{\overline{E}_{FE} = A_{FP}^{-1}[U + R_F \cdot Z_{FF}^{-1}] \cdot \overline{E}_F} \qquad \text{--- A2.2.24}$$

The two Thevenin quantities Z_{FE} and $\overline{E}_{FE}$ are then direct replacements for the original terms R_F and $\overline{E}_F$ calculated for a busbar fault at P.

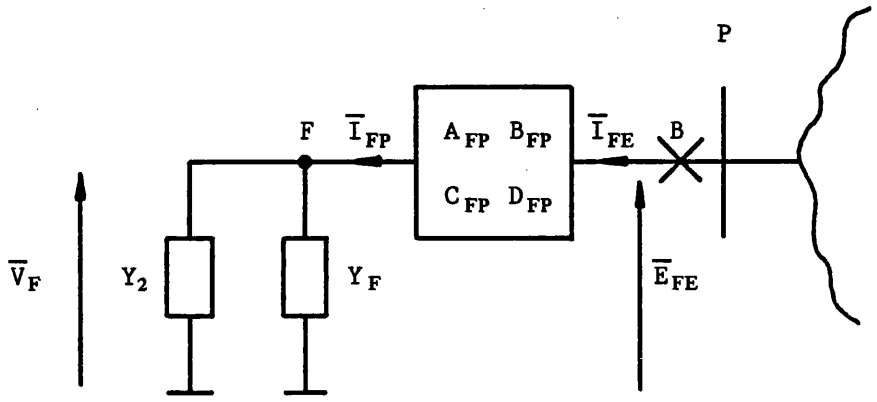


Fig A2.2.1 Two port equivalent circuit for determining Thevenin impedance

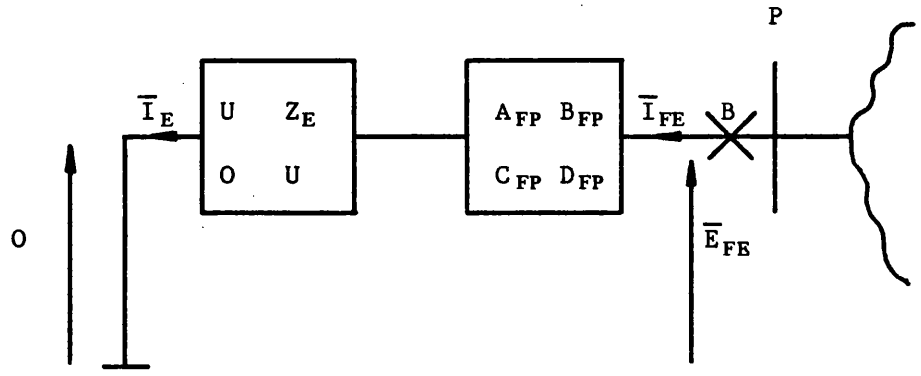


Fig A2.2.2 Equivalent circuit of Fig A2.2.1

APPENDIX A2.3: PARAMETER CONVERSION

In Chapter 2, a two port relationship between the voltages and currents at either end of a homogeneous line section, as shown in Fig 2.2, were developed, such that;

$$\begin{bmatrix} \overline{V}_1 \\ \overline{I}_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} \overline{V}_2 \\ \overline{I}_2 \end{bmatrix} \qquad \text{--- A2.3.1}$$

where $A = [S]\ [\cosh \gamma l]\ [S]^{-1}$

$B = [S]\ [\sinh \gamma l]\ [S]^{-1} Z_O$

$C = Y_O [S]\ [\sinh \gamma l]\ [S]^{-1}$

and $D = Y_O [S]\ [\cosh \gamma l]\ [S]^{-1} Z_O$

An alternative way of relating the same voltage and current components is to derive an equivalent Y parameter matrix (with current $\overline{I}_2$ defined in the opposite direction), such that;

$$\begin{bmatrix} \overline{I}_1 \\ \overline{I}_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} \overline{V}_1 \\ \overline{V}_2 \end{bmatrix} \qquad \text{--- A2.3.2}$$

where $Y_{11} = Y_O [S]\ [\coth \gamma l]\ [S]^{-1}$

and $Y_{12} = -Y_O [S]\ [\operatorname{cosech} \gamma l]\ [S]^{-1}$

For a homogeneous line section as shown in Fig 2.14;

$$Y_{21} = Y_{12}$$

and $$Y_{22} = Y_{11}$$

In cases where the ABCD parameters are derived as combinations of line section and discrete circuit elements such as capacitor banks, homogeneity is then lost and each element of the equivalent Y

parameter matrix must then be defined. Manipulation of Eq A2.3.1 into the form of A2.3.2 yields the following Y parameters in terms of the ABCD equivalents;

$$Y_{11} = D.B^{-1}$$

$$Y_{12} = C - D.B^{-1}.A$$

$$Y_{21} = -B^{-1}$$

and

$$Y_{22} = B^{-1}.A$$

APPENDIX A3.1: THEVENIN SYSTEM IMPEDANCES

For the non-linear capacitor protection analysis, it is necessary to determine the Thevenin impedances presented across the capacitor terminals, both with the fault on and off the system. The following analysis is applicable to single line to ground fault conditions, but is readily extended to cover multi-phase faults.

The universal matrix relationship derived from the de-energised equivalent circuit of the series compensated system, described in Chapter 2 is, for any particular state k, given by;

$$\begin{bmatrix} \overline{E}_F \\ \overline{E}_{CP} \\ \overline{E}_{CQ} \end{bmatrix} = [Z] \begin{bmatrix} \overline{I}_F \\ \overline{I}_{CP} \\ \overline{I}_{CQ} \end{bmatrix} \qquad \text{--- A3.1.1}$$

Inverting Eq A3.1.1 yields an equivalent universal admittance relation of the form;

$$\begin{bmatrix} \overline{I}_F \\ \overline{I}_{CP} \\ \overline{I}_{CQ} \end{bmatrix} = [Y] \begin{bmatrix} \overline{E}_F \\ \overline{E}_{CP} \\ \overline{E}_{CQ} \end{bmatrix} \qquad \text{--- A3.1.2}$$

where $[Y] = [Z]^{-1}$

The latter equation is then expanded into the full three phase expression;

$$\begin{bmatrix} \overline{I}_{Fa} \\ \overline{I}_{Fb} \\ \overline{I}_{Fc} \\ \overline{I}_{CPa} \\ \overline{I}_{CPb} \\ \overline{I}_{CPc} \\ \overline{I}_{CQa} \\ \overline{I}_{CQb} \\ \overline{I}_{CQc} \end{bmatrix} = [Y] \begin{bmatrix} \overline{E}_{Fa} \\ \overline{E}_{Fb} \\ \overline{E}_{Fc} \\ \overline{E}_{CPa} \\ \overline{E}_{CPb} \\ \overline{E}_{CPc} \\ \overline{E}_{CQa} \\ \overline{E}_{CQb} \\ \overline{E}_{CQc} \end{bmatrix} \qquad \text{--- A3.1.3}$$

A3.1.1 Fault On

By consideration of the type of fault, the known zero valued quantities are then substituted into Eq A3.1.3, and for the specific case of an 'a' phase to ground fault;

$\overline{I}_{Fb} = \overline{I}_{Fc} = 0$ and $\overline{E}_{Fa} = 0$ because the circuit is de-energised for the by-pass simulation.

Furthermore, a fault involving only one phase and earth does not result in any by-passing of the capacitors on the healthy phases [8], hence;

$$\overline{I}_{CPb} = \overline{I}_{CPc} = \overline{I}_{CQb} = \overline{I}_{CQc} = 0$$

Therefore, Eq A3.1.3 becomes;

$$\begin{bmatrix} \overline{I}_{Fa} \\ 0 \\ 0 \\ \overline{I}_{CPa} \\ 0 \\ 0 \\ \overline{I}_{CQa} \\ 0 \\ 0 \end{bmatrix} = [Y] \begin{bmatrix} 0 \\ \overline{E}_{Fb} \\ \overline{E}_{Fc} \\ \overline{E}_{CPa} \\ \overline{E}_{CPb} \\ \overline{E}_{CPc} \\ \overline{E}_{CQa} \\ \overline{E}_{CQb} \\ \overline{E}_{CQc} \end{bmatrix} \quad \text{--- A3.1.4}$$

Partitioning and inverting of Eq A3.1.4 yields the following relationship;

$$\begin{bmatrix} \overline{E}_{Fb} \\ \overline{E}_{Fc} \\ \overline{E}_{CPa} \\ \overline{E}_{CPb} \\ \overline{E}_{CPc} \\ \overline{E}_{CQa} \\ \overline{E}_{CQb} \\ \overline{E}_{CQc} \end{bmatrix} = [Z_2] \begin{bmatrix} 0 \\ 0 \\ \overline{I}_{CPa} \\ 0 \\ 0 \\ \overline{I}_{CQa} \\ 0 \\ 0 \end{bmatrix} \quad \text{--- A3.1.5}$$

Where $[Z_2]$ is an 8 x 8 matrix from which a sub-relationship is obtained as follows;

$$\begin{bmatrix} \overline{E}_{CPa} \\ \overline{E}_{CQa} \end{bmatrix} = [Z_T] \begin{bmatrix} \overline{I}_{CPa} \\ \overline{I}_{CQa} \end{bmatrix} \qquad \text{--- A3.1.6}$$

and $[Z_T] = \begin{bmatrix} Z_2(3,3) & Z_2(3,6) \\ Z_2(6,3) & Z_2(6,6) \end{bmatrix}$

Equation A3.1.6 describes the frequency domain relationship between the voltages and currents associated with the capacitor banks at each end of the line. The matrix $[Z_T]$ is of the order 2 x 2 and may be considered as below;

$$[Z_T] = \begin{bmatrix} Z_{T11} & Z_{T12} \\ Z_{T21} & Z_{T22} \end{bmatrix}$$

Where Z_{T11} and Z_{T22} represent the Z_T (w) 'self terms' across the two capacitors and the off diagonal elements represent the transfer impedances necessary for the double by-pass simulation as described in Appendix A3.2.

A3.1.2 Fault Off

Once the current in the fault path is interrupted, ie when the fault path is opened, the Thevenin system impedances presented to the capacitor terminals differ from those calculated above. New constraints are then placed upon Eq A3.1.3 and for the 'a-e' fault condition under consideration;

$$\bar{I}_{Fa} = \bar{I}_{Fb} = \bar{I}_{Fc} = 0$$

and as before, $\bar{I}_{CPb} = \bar{I}_{CPc} = \bar{I}_{CQb} = \bar{I}_{CQc} = 0$

In this case however, Eq A3.1.1 is relevant, since all fault path currents are zero, hence;

$$\begin{bmatrix} \bar{E}_{Fa} \\ \bar{E}_{Fb} \\ \bar{E}_{Fc} \\ \bar{E}_{CPa} \\ \bar{E}_{CPb} \\ \bar{E}_{CPc} \\ \bar{E}_{CQa} \\ \bar{E}_{CQb} \\ \bar{E}_{CQc} \end{bmatrix} = [Z] \begin{bmatrix} 0 \\ 0 \\ 0 \\ \bar{I}_{CPa} \\ 0 \\ 0 \\ \bar{I}_{CQa} \\ 0 \\ 0 \end{bmatrix} \qquad \text{--- A3.1.7}$$

Such an expression is partitioned directly to give;

$$\begin{bmatrix} \bar{E}_{CPa} \\ \bar{E}_{CQa} \end{bmatrix} = [Z_T] \begin{bmatrix} \bar{I}_{CPa} \\ \bar{I}_{CQa} \end{bmatrix} \qquad \text{--- A3.1.8}$$

where $[Z_T] = \begin{bmatrix} Z(3,3) & Z(3,6) \\ Z(6,3) & Z(6,6) \end{bmatrix}$

The latter expression is in exactly the same form as Eq A3.1.6 with the elements of $[Z_T]$ now modified as a result of the fault break off.

APPENDIX A3.2: DOUBLE NON-LINEAR CAPACITOR BY-PASSING

The time domain solution of the non-linear resistor voltage associated with the protection equipment of one capacitor was derived from the frequency domain voltage balance equation below;

$$\overline{V}_R = \overline{E}_C - Z_T . \overline{I} \qquad \text{--- A3.2.1}$$

As explained in Chapter 3, Section 3.2.3, the non-linear path is momentarily opened at the instant at which the second capacitor voltage exceeds the threshold level, redefining the time datum to zero at this instant. Hence two equal and opposite forcing functions $e_{CP}(t)$ and $e_{CQ}(t)$ are then supplied simultaneously to the de-energised network. The frequency domain relationship between the two capacitors may be expressed as;

$$\begin{bmatrix} \overline{V}_{RP} \\ \overline{V}_{RQ} \end{bmatrix} = \begin{bmatrix} \overline{E}_{CP} \\ \overline{E}_{CQ} \end{bmatrix} - [Z_T] \begin{bmatrix} \overline{I}_{RP} \\ \overline{I}_{RQ} \end{bmatrix} \qquad \text{--- A3.2.2}$$

hence the voltages and currents at either end are interdependent with $[Z_T]$ being a 2 x 2 matrix, the elements of which being dependent upon the fault condition, as explained in Appendix A3.1. Once again, since $\overline{V}_{RP}$ and $\overline{V}_{RQ}$ may only be related to $\overline{I}_{RP}$ and $\overline{I}_{RQ}$ in the time domain, it is necessary to firstly expand Eq A3.2.2 and then to transform the latter into a time domain equivalent. Writing Eq A3.2.2 in full;

$$\overline{V}_{RP} = \overline{E}_{CP} - Z_{T11} . \overline{I}_{RP} - Z_{T12} . \overline{I}_{RQ}$$
$$\text{and} \quad \overline{V}_{RQ} = \overline{E}_{CQ} - Z_{T21} . \overline{I}_{RP} - Z_{T22} . \overline{I}_{RQ} \qquad \text{--- A3.2.3}$$

Using the same procedure as for the single by-pass case, the time domain equivalent equations for Eq A3.2.2, on a discrete sample by sample basis are then;

$$v_{RP}(n) = e_{CP}(n) - [C_{11}.i_{RP}(n) + D_{11} + X_{11}] - [C_{12}.i_{RQ}(n) + D_{12} + X_{12}]$$

and $$v_{RQ}(n) = e_{CQ}(n) - [C_{21}.i_{RP}(n) + D_{21} + X_{21}] - [C_{Q2}.i_{RQ}(n) + D_{22} + X_{22}] \quad \text{--- A3.2.4}$$

where $C_{11} = Z_{T11}(o).\Delta T/2$, $C_{12} = Z_{T12}(o).\Delta T/2$, etc

$D_{11} = Z_{T11}(n).i_{RP}(o).\Delta T/2$, $D_{12} = Z_{T12}(n).i_{RQ}(o).\Delta T/2$, etc

and $$X_{11} = \sum_{k=1}^{n-1} Z_{T11}(n-k).i_{RP}(k).\Delta T ,$$

$$X_{12} = \sum_{k=1}^{n-1} Z_{T12}(n-k).i_{RQ}(k).\Delta T, \text{etc}$$

Considering the non-linear characteristics;

$$v_{RP}(n) = V_{CP} + m_P.i_{RP}(n)$$

and $$v_{RQ}(n) = V_{CQ} + m_Q.i_{RQ}(n), \quad \text{--- A3.2.5}$$

which when subtituted into Eq A3.2.4 gives;

$$V_{CP} + m_P.i_{RP}(n) = e_{CP}(n) - [C_{11}.i_{RP}(n) + D_{11} + X_{11}] - [C_{12}.i_{RQ}(n) + D_{12} + X_{12}]$$

and $$V_{CQ} + m_Q.i_{RQ}(n) = e_{CQ}(n) - [C_{21}.i_{RP}(n) + D_{21} + X_{21}] - [C_{Q2}.i_{RQ}(n) + D_{22} + X_{22}] \quad \text{--- A3.2.6}$$

To aid the understanding of the solution of the above equations, the first sample is considered, at which the following variables are known to be zero;

$$V_{CP}, V_{CQ}, X_{11}, X_{12}, X_{21} \text{ and } X_{22}$$

hence;

$$m_P \cdot i_{RP}(1) = e_{CP}(1) - C_{11} \cdot i_{RP}(1) - D_{11} - C_{12} \cdot i_{RQ}(1) - D_{12}$$

and $$m_Q \cdot i_{RQ}(1) = e_{CQ}(1) - C_{21} \cdot i_{RP}(1) - D_{21} - C_{22} \cdot i_{RQ}(1) - D_{22}$$

--- A3.2.7

In Eq A3.2.7, C_{11}, .. , C_{22} and D_{11}, .. , D_{22} are constants and the initial values of m_P and m_Q are pre-determined from the non-linear resistor characteristic. With two known quantities, e_{CP} (1) and e_{CQ} (1), the equation is solved simultaneously for $i_{RP}(1)$ and $i_{RQ}(1)$, from which the corresponding values of $v_{RP}(1)$ and $v_{RQ}(1)$ are obtained. Thus the recursive process is initiated with the first current samples becoming the past history values, necessary for determining the constants X_{11}, X_{12}, X_{21} and X_{22} for the second sample. This enables the solution of Eq A3.2.6 for any sample, n. The time domain variations of e_{CP}, e_{CQ}, v_{RP} and v_{RQ} are then calculated for the entire observation period, enabling the modified frequency domain forcing voltages to be found.

APPENDIX A7.1: 500 kV SYSTEM PARAMETERS

The conductor arrangements for the single and double circuit systems considered are as indicated in Fig A7.1. The distances of the conductors above ground are average values taking into account the catenary of the span between two consecutive towers. For both systems, an earth plane resistivity of 100 Ω.m was assumed and due to the horizontal construction, the material of the earth wires is Alumoweld, which is known to be approximately 25 times more resistive than ACSR phase conductors. The following power frequency (50 Hz) parameters are then applicable;

(A) Single Circuit System

Phase conductor resistance = 0.0339 Ω/km

Phase conductor reactance = 0.0078 Ω/km

Phase conductor radius = 9.05 cm

(Two conductors per phase)

Earth wire resistance = 1.882 Ω/km

Earth wire reactance = 0.388 Ω/km

Earth wire radius = 1.8 cm

The above parameters, together with the tower arrangements and earth plane effects, produce the following parameters;

Self impedance $Zs = 0.122 + j0.54\ \Omega/km$

Mutual impedance $Zm = 0.088 + j0.22\ \Omega/km$

Self admittance $Ys = j0.354.10\ \Omega^{-1}/km$

Mutual admittance $Ym = j0.298.10\ \Omega^{-1}/km$

PPS impedance $Z1 = Zs - Zm$

$= 0.034 + j0.32\ \Omega/km$

ZPS impedance $Z0 = Zs + 2.Zm$

$= 0.298 + j0.98\ \Omega/km$

PPS admittance $Y1 = Ys + Ym$

$= j0.384.10\ \Omega^{-1}/km$

ZPS admittance $Y2 = Ys - 2.Ym$

$= j0.299.10\ \Omega^{-1}/km$

Aerial mode surge impedance,

$$Z_{02,3} = 283\ \Omega$$

Earth mode surge impedance,

$$Z_{01} = 579\ \Omega$$

(B) Double Circuit System

Phase conductor resistance = 0.017 Ω/km

Phase conductor reactance = 0.0039 Ω/km

Phase conductor radius = 13.3 cm

(Four conductors per phase)

Earth wire resistance = 1.76 Ω/km

Earth wire reactance = 0.408 Ω/km

Earth wire radius = 1.15 cm

The above parameters, together with the tower arrangements and earth plane effects, produce the following parameters.

Self impedance $Zs = 0.032 + j0.41\ \Omega/km$

Mutual impedance $Zm = 0.015 + j0.11\ \Omega/km$

Self admittance $Ys = j0.34.10\ \Omega^{-1}/km$

Mutual admittance $Ym = j0.41.10\ \Omega^{-1}/km$

PPS impedance $Z1 = Zs = Zm$

$= 0.017 + j0.3\ \Omega/km$

ZPS impedance $Z0 = Zs + 2.Zm$

$= 0.062 + j0.63\ \Omega/km$

PPS admittance $Y1 = Ys + Ym$

$= j0.381.10\ \Omega^{-1}/km$

ZPS admittance $Y2 = Ys - 2.Ym$

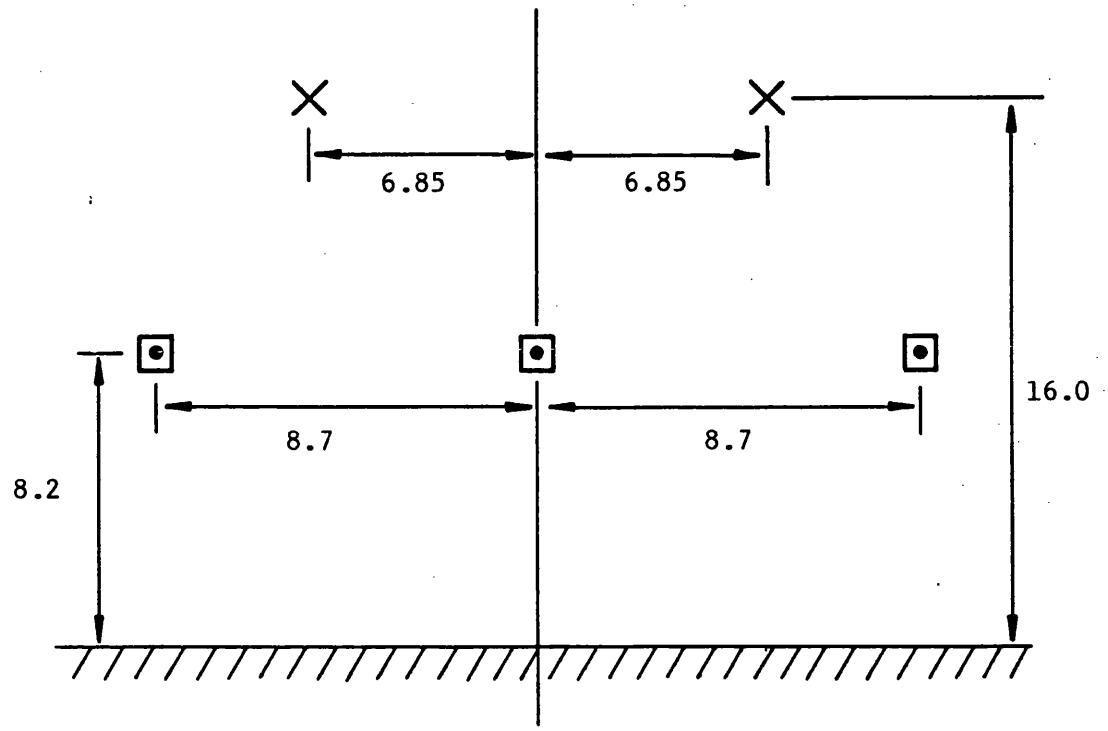
$= j0.258.10\ \Omega^{-1}/km$

Aerial mode surge impedance,

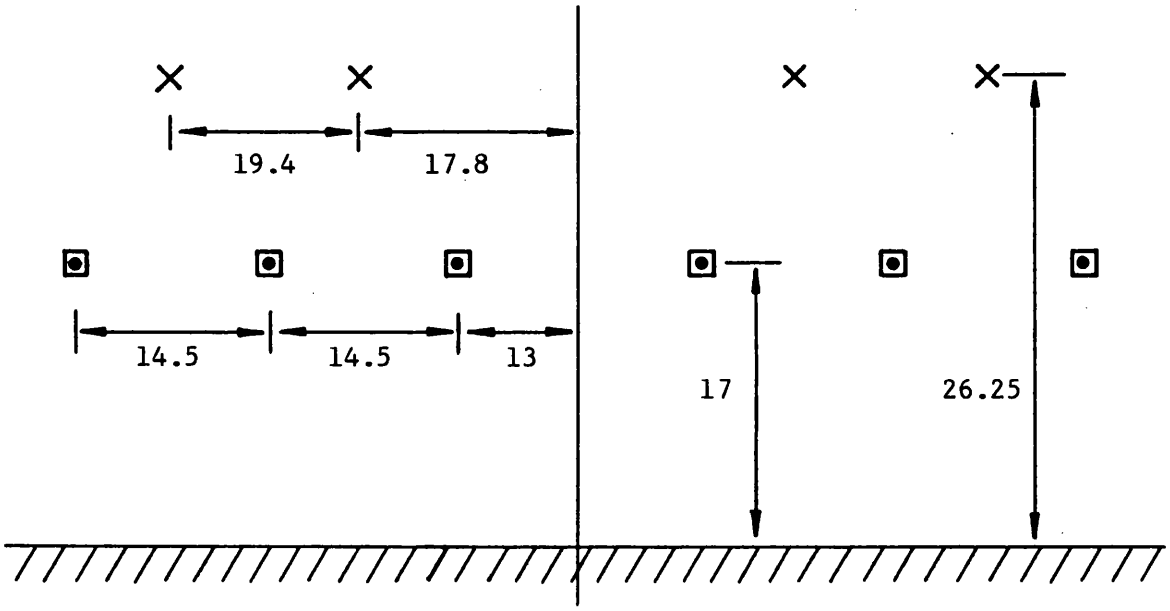
$$Z_{02,3} = 280\ \Omega$$

Earth mode surge impedance,

$$Z_{01} = 495\ \Omega$$



(a) Single circuit horizontal construction



(b) Double circuit horizontal construction

⊡= phase conductors X= earth wires

Fig A7.1 Tower conductor arrangements for single and double circuit systems. (Dimensions in metres)

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20th Universities' Power Engineering Conference
on 4 April 1985.

THE APPLICATION OF A NEW DIRECTIONAL COMPARISON PROTECTION SCHEME TO CAPACITOR COMPENSATED EHV TRANSMISSION SYSTEMS

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ABSTRACT

A new Directional Comparison Protection Scheme as applied to series compensated lines is described. The principles on which the scheme is based utilise superimposed values of the modal voltages and currents at the line ends. The special techniques developed overcome the longstanding problems (due primarily to capacitor gap flashovers), of adequately protecting series compensated lines and provide a performance which satisfies the requirements for reliable and secure protection of such lines.

INTRODUCTION

The use of series compensated lines in long-distance ac transmission practice is well known. There are, however, problems encountered in the protection of such lines and these arise primarily as a result of the rapid circuit parameter changes due to the operation of various capacitor spark gaps protecting the capacitors against overvoltages. This, in turn, causes rapid changes in the measured effective system impedance, thus affecting the performance of conventional protection relays. However, some of the recently developed ultra-high-speed (UHS) protection equipments offer much promise in solving the longstanding problems of providing an adequate and reliable protection for long-distance series compensated lines. This is particularly so in view of the fact that the speed of operation of such equipments, coupled with their new principles of operation (different from those of conventional equipments), makes them immune to the effects caused by capacitor gap flashover.

In this paper, the basis of a new UHS directional comparison protection scheme, based upon the concept of measuring from superimposed component measurands, is described. The scheme is designed to operate in a blocking mode in conjunction with a carrier communication channel. Particular emphasis is placed on outlining the special filtering and signal processing arrangements which have been developed to achieve relay dynamic stability under external faults without affecting the UHS fault detection capability of the relay, this being irrespective of whether there is capacitor gap flashover(s) or not.

The paper concludes by presenting some interesting results relating to a typical 500kV series compensated long line application.

RELAY OPERATING PRINCIPLES

The basic relay operating principle relies upon deriving two signals A(t) and B(t) using the superimposed values of modal voltages and currents at each end of a feeder. In this respect it should be noted that some economy is gained by forming signals proportional only to the Aerial modes of voltages and currents (modes 1 and 2) [1], as this requires the processing and transmission of only two

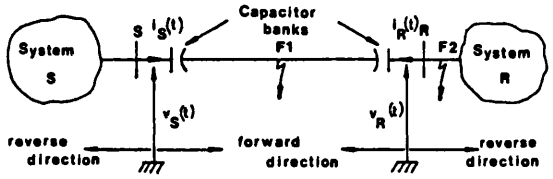


Fig. 1. Simple line interconnection.

signal components. With reference to Fig.1, the two signals A(t) and B(t) (for each mode) at ends S and R are of the form:

$$A_{1,2}(t) = K.v_{1,2}(t) - i_{1,2}(t).R_o$$
$$B_{1,2}(t) = K.v_{1,2}(t) + i_{1,2}(t).R_o \quad \ldots (1)$$

where K = voltage scaling constant
R_o = replica resistance matched to the line surge impedance Z_o
v,i = superimposed modal quantities at line ends

As described by Johns [2], the criteria for determining the direction to fault is based on the fact that, for an internal fault (at F1), the modal voltage and current components at each end are in anti-phase, resulting in $|A(t)| > |B(t)|$ and hence giving forward fault indication by both relays. For an outer zone fault (say at F2) on the other hand, although the relay at end S would still indicate a forward fault, the modal voltage and current components at end R are co-phasal, resulting in $|B(t)| > |A(t)|$, i.e. a reverse fault indication, thus preventing a breaker trip at both ends.

It should be noted that, in practice, it is necessary to compare the magnitude differences of the two signals over a number of samples before a trip or block decision is made. Furthermore, an extensive series of studies has shown that the magnitude differences of the two signals in the initial measuring period are very much a function of the fault inception angle, and hence it is necessary to also check the difference in the rate of change of the two signals. Moreover, before the decision process is initiated, both of the aforementioned difference functions must exceed a preset minimum threshold level, a feature which has been incorporated to increase relay security in the presence of system noise.

RELAY DESCRIPTION

The methods for deriving the total variations of the modal components from the primary system voltages and currents are as described in reference 2. Fig.2 shows a block schematic of the digital processes associated with the relay at each end of the feeder. The superimposed extraction filter comprises two units, one of half cycle and the other of full cycle of nominal power frequency delay. The first sub-filter provides exactly the superimposed component for one half cycle. The full cycle

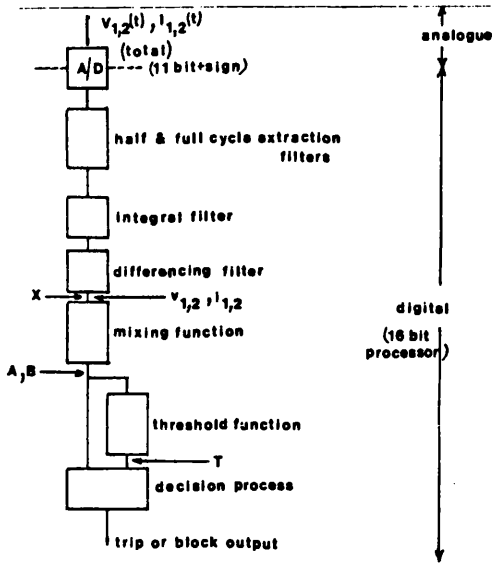


Fig. 2. Schematic of the digital processes.

extractor, together with the integral and differencing filters, essentially aid in the rejection of high frequency and dc offset components in the signals once a decision has been made, thus improving the relay recovery capability.

During steady state conditions the threshold rests at its minimum level, thus maximising relay sensitivity. Upon fault inception, however, a delaying action restrains any threshold increase to allow for the relay to render a decision, after which the threshold becomes solely dependent upon the signal behaviour.

It should be noted that, unlike with plain feeders, in series compensated lines there can be present some residual subsynchronous components in the relaying signals for many cycles after fault inception, particularly for external faults. It has been found that the frequency of these components is typically in the range of 10 to 40 Hz. For the relay described here, the threshold function is therefore adapted such that the threshold level is maintained well above the relay measurands during resonant conditions in order to prevent any relay mal-operation.

RELAY RESPONSE STUDIES

All the results presented are for the typical 500KV horizontally constructed single circuit line application shown in Fig.3. The simulation techniques for accurately generating the fault transient waveforms are as described in reference 3. The series capacitor protection equipment has been modelled for the more widely used single gap schemes. In this respect it should be noted that any damping elements have been deliberately omitted from the capacitor protection scheme model so as to admit the severist switching transients into the waveforms. The capacitor protection equipment is then represented by a simple open/close switch as shown in Fig.3.

Relay Performance for Internal Faults

Figs.4a-h show the outputs of the different processes (for relay at end S) generated under a typical fault condition. As mentioned previously, once the total modal voltage and current components have been formed using the primary system phase voltages and currents (Figs.4a and 4b), the analogue

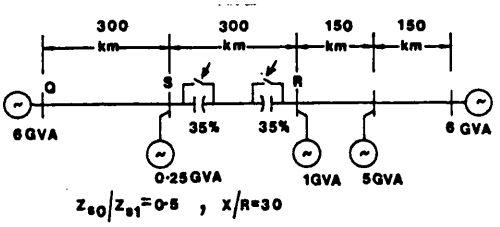


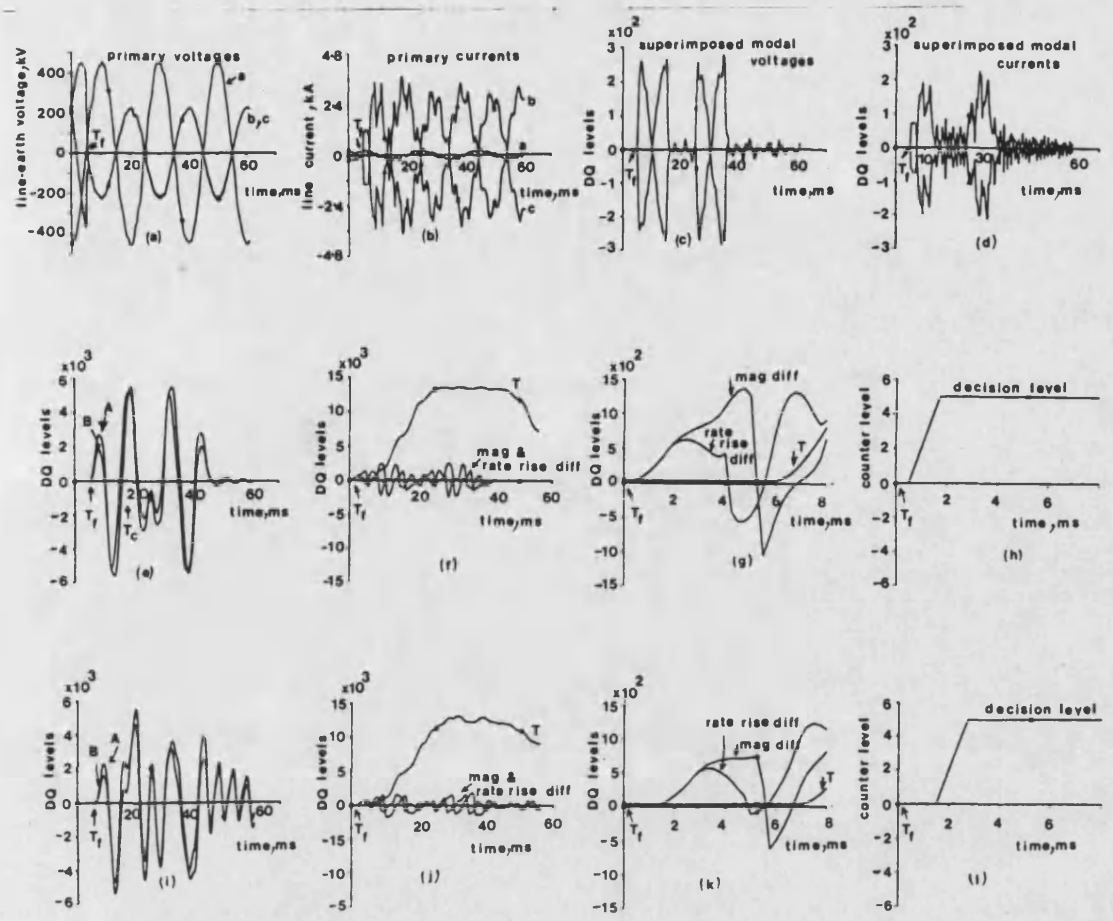
Fig. 3. System configuration studied.

signals are first converted into digital form. The outputs of the extraction filters (point X in Fig.2) are as shown in Figs.4c and 4d. The filter arrangement is such that it gives the correct superimposed output for only half a cycle of power frequency after a disturbance, this period being more than adequate for the relay to make a decision. When considering the two relay measurands, Fig.4e clearly shows that, for the fault condition considered, the magnitude of signal A is greater than that of signal B in the initial measuring period. This results in both the magnitude and rate of rise differences between the two measurands to be well above the variable threshold level T during the measuring period, as evident firstly from Fig.4f and then more clearly from the detailed waveforms of Fig.4g. The decision counter quickly attains the required positive level for a forward fault indication as shown by Fig.4h. Also noticeable from Fig.4t is the sharp rise in the dynamic threshold once the initial decision has been made. It should be noted that, although not shown here, the relay performance at end R for the fault condition considered is almost identical to that at end S.

Figs.4i-l show the signal waveforms for an internal fault remote from end S. Here again, it can be clearly seen that the relay at end S (and also the end R relay) gives a correct decision with operating times similar to that for the close up fault condition considered previously. Comparing Figs.4e and 4i, it is interesting to note that, whilst in the former case the two signals tend to zero approximately 2.5 cycles after fault inception, in the latter case they persist for a much longer period. This phenomenon can be directly attributed to the fact that for the close up fault both the capacitors flashover whereas for the remote end fault they stay in the circuit, thus introducing subsynchronous components into the measurands.

Relay Performance for External Faults

When considering the end S relaying signals for a close up fault just behind the end S relay, Fig.5a shows that this time it is the magnitude of signal B which is greater than that of A in the initial measuring period. It is clearly evident from Figs.5b and 5c that both the magnitude and rate differences exceed the negative threshold level, thus making the counter attain a negative decisive value (Fig.5d), resulting in the relay giving a reverse fault indication. As expected, the relay measurands A and B for the end R relay produce magnitude and rate differences which, having exceeded the positive threshold level, force the counter and hence the relay to indicate a forward fault (Figs.5e and 5f). Looking at Figs.5a and 5b, it is interesting to note that, once the relay measurands have gone to near zero, the reverse fault break off (approx. 2 cycles after fault) and the subsequent reinsertion of the two capacitors (approx. 200ms after fault) introduce extremely small transient components into the measurands, thus keeping both the magnitude and rate differences well below the threshold level (Fig.5b). This importantly indicates that, as desired, the relay is immune to such circuit changes and responds only



b-c phase fault at $V_{bcg0}°$, (a)-(h)=fault near end S, (i)-(l)=fault near end R, model signals, waveforms for end S relay, DQ=digital quantisation, T_f=fault inception, T_c=capacitor gaps sparkover

Fig. 4. Relay signals for internal faults.

to faults on the line. Furthermore, it can also be seen that the threshold level resets approx. 220ms after fault.

Figs.5g-l show the relaying signals at ends S and R for a remote end reverse fault (from end S) in which both the capacitors stay in the circuit. Here again, it is clearly seen that both the relays give a correct decision, i.e. a reverse fault indication by end S relay and a forward fault indication by end R relay.

It should be noted that, although the relay performance has been examined here for a limited number of fault studies only, an extensive series of studies has shown that the relay gives correct UHS performance for all forward and reverse fault conditions irrespective of whether there is capacitor gap flashover(s) or not.

CONCLUSIONS

In this paper the basic principles and implementation of a new directional comparison relay as applied to series compensated ehv lines has been outlined. The results presented clearly show that the relay gives correct UHS performance for both forward and reverse faults. It is particularly shown that the special techniques developed make the relay immune to the fault break off and capacitor reinsertion transients under external fault conditions. In addition, they minimise the relay recovery time following an external fault, thus permitting the detection of any subsequent faults with minimum delay.

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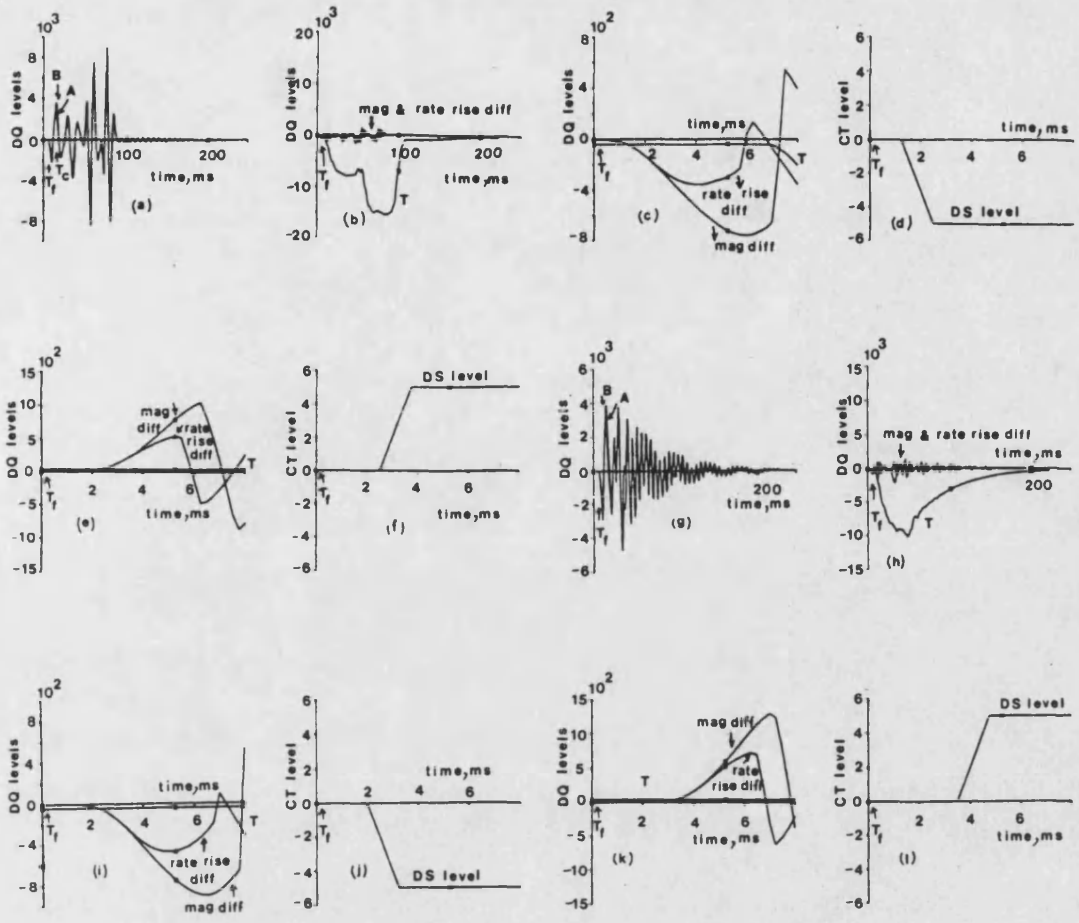

a-earth fault at v_{a0}, mode 2 signals, (a)-(f)=fault near end S, (a)-(d)=end S relay, (e)-(f)=end R relay, (g)-(l)=fault at Q (fig 3), (i)-(j)=end S relay, (k)-(l)=end R relay, DQ=digital quantisation, CT=counter, DS=decision, T_f=fault inception, T_c=capacitor gaps sparkover

Fig. 5. Relay signals for external faults.

The following paper has been sent

to the IEEE for consideration.

THE DEVELOPMENT AND APPLICATION OF DIRECTIONAL COMPARISON PROTECTION FOR SERIES COMPENSATED TRANSMISSION SYSTEMS

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Abstract - A new high speed Directional Comparison protection relay for capacitor compensated lines is described. It is shown that the special filtering and signal processing techniques developed overcome many difficult protection problems encountered on such lines. The relay design, although based on CAD methods, can be readily implemented using present generation hardware.

INTRODUCTION

Series compensated transmission lines often pose difficult protection problems and, for this reason, they commonly require careful application studies [1,2]. Any mode of independent tripping, without the concurrent use of signalling channels linking the protection at the two ends, is often unsatisfactory. For example, Distance relays can, depending on their settings, either overreach or underreach as a direct consequence of the operation of the series capacitor protection arrangements which, in general, do not conform to any pre-defined pattern [3].

One very common method of protecting series compensated lines involves the use of Distance relays operating in a directional comparison mode in conjunction with either carrier or microwave signalling channels. However, even with this arrangement, it is not uncommon to encounter problems caused by a loss of directionality arising as a result of voltage reversal at the relay location. This is particularly so in systems where the capacitors are located at the line ends and the system is subjected to a low level fault that does not cause capacitor protection gap flashover. Another noteworthy problem concerns double circuit applications where, under some fault conditions, the presence of the second circuit can cause the voltage or current on a faulted line to reverse and thereby initiate blocking under internal fault conditions.

The foregoing considerations account, to a large extent, for ongoing interest in the development of alternative and improved methods of protection for series compensated systems. In this respect, recent years have seen the emergence of Directional Comparison schemes in which the directional decision is initiated by relays of the travelling wave type [4,5]. It was against the above described background that work commenced on the application of the Directional Comparison scheme, originally developed for application to plain feeders, described in references [6] and [7]. The primary purpose of this paper is thus to outline progress made in the further design, development and application of the latter to series compensated systems.

Particular emphasis has been placed on producing a design that not only overcomes the foregoing practical problems but which also addresses a number of other potential problems in the application of high speed Directional Comparison schemes to series compensated systems. In this respect, particular attention has been paid to designing the new equipments so that the reset time of the relays is reduced to an acceptable level, thereby maximising the ability of the relays to respond to faults which are closely preceded by faults external to the protected line. This is of particular importance in applications where subsynchronous resonance components induced by faults external to the protected line may delay resetting of the protection. Another potential problem concerns the situation where a high level fault external to the protected line causes capacitor protection gaps to flashover which, in turn, cause a disturbance which appears internal to the protected line. Similar problems can arise following capacitor reinsertion.

The paper describes the special filtering and signal processing schemes that have been developed to satisfactorily deal with the foregoing problems. Programmable based methods have been used to assess the relay performance which is illustrated by reference to the results of some of the more interesting studies in typical 500kV, 60Hz series compensated applications having dual gap protection arrangements [8].

RELAY OPERATING PRINCIPLES

The basic relay operating principle relies upon deriving two composite superimposed signals S1(t) and S2(t) using modal voltages and currents at each end of a feeder. In this respect it should be noted that the use of modal quantities eliminates the mutual coupling between the phases of a transmission line thus minimising the error which results from applying a Directional Comparison scheme on a phase by phase basis. The two modal components (modes 2 and 3) used here are based on the transformation as used in reference [7] and

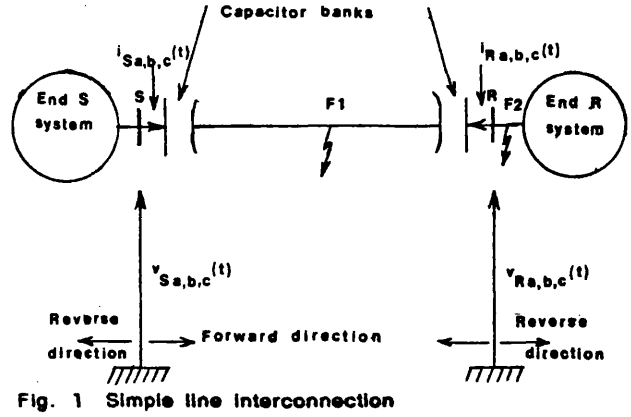


Fig. 1 Simple line interconnection

are suitable for all practically encountered faults.

With reference to the simple diagram of Fig. 1. the modal voltage and current components (the derivation of which is shown later) at say. end S. are of the form:

$$v_{s2}(t) = v_{sa}(t) - v_{sb}(t);\ i_{s2}(t) = i_{sa}(t) - i_{sb}(t)$$

$$v_{s3}(t) = v_{sa}(t) - v_{sc}(t);\ i_{s3}(t) = i_{sa}(t) - i_{sc}(t) \quad \ldots(1)$$

The two corresponding signals S1(t) and S2(t) are then given by:

$$S1_{2,3}(t) = v_{s2,3}(t) - Ki_{s2,3}(t)$$

$$S2_{2,3}(t) = v_{s2,3}(t) + Ki_{s2,3}(t) \quad \ldots(2)$$

where K = positive scaling resistance constant and is taken as being = R_0. the real approximation of the line surge impedance.

The two signals. S1(t) and S2(t). are nominally zero under normal system operating conditions and become finite only when a disturbance occurs. As outlined in reference [7]. the criteria for determining the direction to fault is based on the fact that for an internal fault (at. say. F1). the superimposed modal voltage and current components are of opposite polarities at each end of the feeder resulting in:

$$|S1(t)| > |S2(t)| \quad \ldots(3)$$

A forward fault indication is thus given by both relays. Conversely. for an out-of-zone fault (at. say. F2). although the relay at end S gives a forward fault indication. however. the modal voltage and current components at end R are of like polarity resulting in:

$$|S2(t)| > |S1(t)| \quad \ldots(4)$$

A reverse fault indication is thus given by the relay at end R and a block signal is initiated. A point to note here is that the directional criteria shown in eqns (3) and (4) are true whatever the magnitude of the constant K in eqn (2) [7].

In order to improve relay security. it is necessary to compare the magnitude differences between the signals S1(t) and S2(t) over several consecutive samples. In this respect it should be mentioned that special digital filters (as later described in detail) are used in the relay design to provide the signals S1(t) and S2(t) of correct polarities for an extended time after fault. Care needs also to be taken for fault conditions (such as faults near voltage zero) where. in spite of the filtering. the criteria of eqns (3) and (4) are valid only for a very short period following fault inception. Hence it is also necessary to compare the rate differences of the two signals. The magnitude and rate difference functions used are described as:

$$DM = |S1| - |S2|$$

$$DR = |S1'| - |S2'| \quad \ldots(5)$$

Finally. in order to prevent the relay responding to any spurious system noise. both the aforementioned difference functions must exceed a preset minimum threshold level.

RELAY DESCRIPTION

The Directional Detection relay described herein is a hybrid relay comprising analogue and digital parts. The former of the two is concerned with the derivation of the total (steady-state and superimposed) variations of modal components from the primary system voltages and currents at a feeder end and the methods adopted for this part are essentially the same as those outlined in reference [7]. A sampling frequency (f_s) of 4.8kHz provides a satisfactory response and an investigation has shown that this would not impose any undue demand on hardware requirements. An analogue prefilter with a second-order low pass Butterworth characteristic and a 2kHz cut-off frequency ensures no aliasing. The adjustable gains on the voltage and current interfaces in the analogue part are such as to make the relay setting procedures for a particular application. simple and straightforward.

Digital Processing

The digital part comprises filters and a decision process. The filter arrangement. as shown in a block schematic in fig. 2. has been specifically designed both

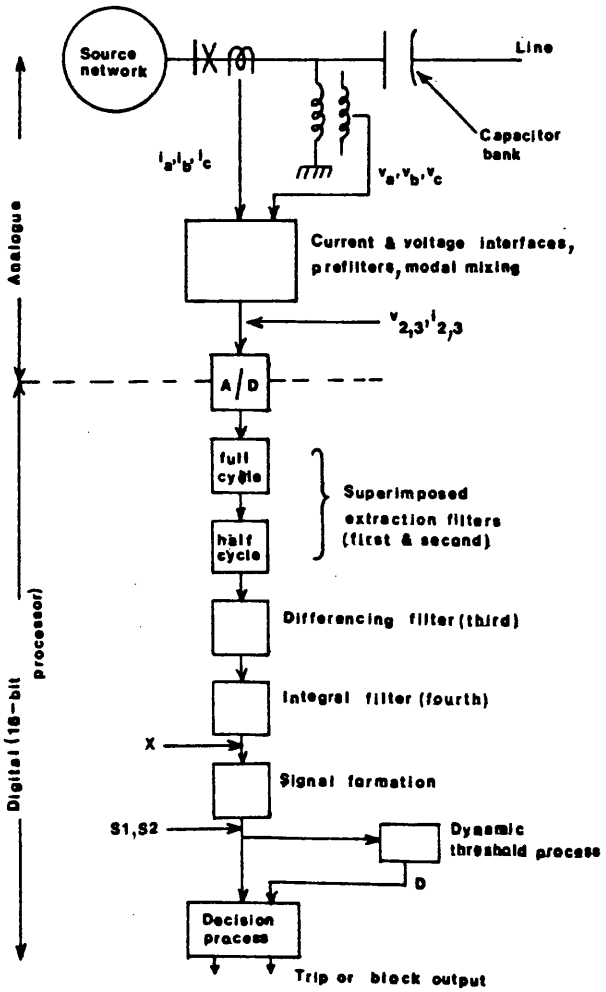


Fig. 2 A block schematic of the complete scheme

to provide rapid relay response for high speed (HS) fault detection (i.e. directional determination in say typically 4ms) and a fast relay recovery. subsequently. It comprises four filters. the first two for extracting the superimposed components from the total input signals and the second two for reducing the relay recovery time.

The superimposed extraction filters provide the transient components by rejecting the steady-state power frequency components from the total variations of signals. In this respect, a full scale CAD study has revealed that it is desirable to employ a cascaded arrangement comprising full cycle and half cycle extraction filters. Such an arrangement provides the exact superimposed component for half a cycle of power frequency after a disturbance and has a frequency response which makes the relay virtually immune to errors caused by frequency drifts of up to ±5% in the nominal power frequency. For a 60Hz system, the two combined filters have a Z-plane transfer function given by:

$$T_1(Z) = (1-Z^{-80})(1+Z^{-40}) \quad \ldots(6)$$

where $Z^{-1} = \exp[-jw\Delta T]$, $\Delta T = \frac{1}{f_s} = 0{\cdot}2083\text{ms}$.

As mentioned before, the primary purpose of the third and fourth filters is to reduce the time taken by the relay to recover its ability to protect the line subsequent to a previous fault. In addition, these filters also minimise the possibility of relay mal-operation due to any transitory signal sign reversals during the immediate post-fault period. The third filter has a very high low-frequency rejection capability and is specifically designed to reduce the relay recovery time both in the presence of any significant exponential offset components in the measurands (such as for voltage minimum faults) and any subsynchronous resonance components particularly in cases where a fault level is not high enough to cause capacitor gap flashover. The transfer function of the filter is given by:

$$T_2(Z) = (1-Z^{-20})^2 \quad \ldots(7)$$

The impulse response of the filter is such that it passes without any distortion, the superimposed components generated by the previous two filters for 1/4 cycle of power frequency, i.e. for 4.16ms.

The main purpose of the fourth filter, which has a low pass characteristic, is to improve the relay recovery time by significantly reducing the high frequency components for a fault near voltage maximum. In this respect it should be mentioned that because of the long line lengths associated with series compensated systems, the lowest travelling wave frequency can be such that its total rejection would require a much higher order filter than that for an uncompensated system and this can cause a significant increase in the relay operating time. The design of this filter is thus a compromise between the conflicting requirements of HS relay operation and a short relay recovery time. The filter implemented has a transfer function given by:

$$T_3(Z) = [(1-Z^{-(m+1)})/(1-Z^{-1})]^2 \quad \ldots(8)$$

where m = integer number.

The value of m in eqn (8) is dependent upon the lowest dominant travelling wave frequency (f_t) which, in turn, depends on the system configuration. For example, for a 300km series compensated line terminated in low capacity sources (this being generally the case in practical series compensated systems), it can be shown that $f_t \approx 250$Hz. The value of m is adjusted such that the first zero gain of the filter occurs at a frequency just below f_t. Thus for the system considered, m is given by the nearest integer to the value:

$$\left[\frac{1}{f_t.\Delta T} - 1\right] = \frac{1}{(250.0 \cdot 2083.10^{-3})} - 1 \quad \ldots(9)$$

i.e. m = 18

Dynamic threshold process: As mentioned previously, before the relay can render a decision, both the magnitude and rate differences of the two signals S1 and S2 have to be compared in a specially designed decision process. A detailed description of the latter, which comprises a bi-directional counter which is incremented for forward detection and decremented for reverse detection, is given in reference [7]. With regard to the threshold level, once the relay has made the initial decision as to the direction of fault, it must stay above the relay measurands until such time as the latter have died down. This requirement which ensures relay stability and which is particularly important for external faults and faults close to the relay sensitivity level, has been achieved by designing a dynamic threshold process (fig. 2). In this process, the threshold signal D (as described in a general form by eqn (10)) takes a moving average of the two relaying signals S1 and S2 over a system dependent period of time.

$$D(n) = K_0 + 1/N \sum_{k=k_1}^{k=k_2} |S1(n-k)| + |S2(n-k)| \quad \ldots(10)$$

where K_0 = minimum preset level, and is chosen as = 40 levels

As shown in the above equation, an initial delay T_d (where $T_d = k_1.\Delta T$) has been incorporated to maximise the relay sensitivity in the initial fault detection period. For the relay described here, T_d corresponds to 1/4 cycle of power frequency, i.e. $k_1 = 20$. The value of k_2 and, therefore, the moving average window width is dependent upon the expected subsynchronous resonance frequency f_r which, in turn, is very much a function of both system and fault conditions. However, consideration of the overall response of the filtering stages has revealed that the dynamic function D should be based upon an assumed steady-state frequency approximately half that of the nominal power frequency, i.e. f_r = 30Hz in this case. Furthermore, it has been found that if the above mentioned window width is set to be approximately equal to half the periodic time of frequency f_r, then the threshold signal D always stays well above the measurands until such time as the latter have died down, whereby D then quickly returns to its minimum preset level. Thus, for the system considered, k_2 is given by the nearest integer to the value:

$$\frac{1}{2f_r.\Delta T} + k_1 = \frac{1}{2.30.0 \cdot 2083.10^{-3}} + 20 \quad \ldots(11)$$

i.e. $k_2 = 100$

The integer N in eqn. (10) is defined as $N = (k_2 - k_1)/2 = 40$. However, for ease of digital division, N is taken as 32.

A dynamic threshold process of this nature thus provides a near optimum performance in that: a) the relay retains its maximum sensitivity in the initial fault detection period; and, b) any relay mal-operation is prevented from occurring during the entire period that the signals are finite.

SYSTEM PARAMETERS

The relay performance has been examined for different systems. The majority of results presented are for a typical 500kV horizontally constructed single line application. The arrangements for this system are as shown in Figs. 3(a) and 3(b). A limited study showing the relay performance in double circuit line applications is also presented using the typical

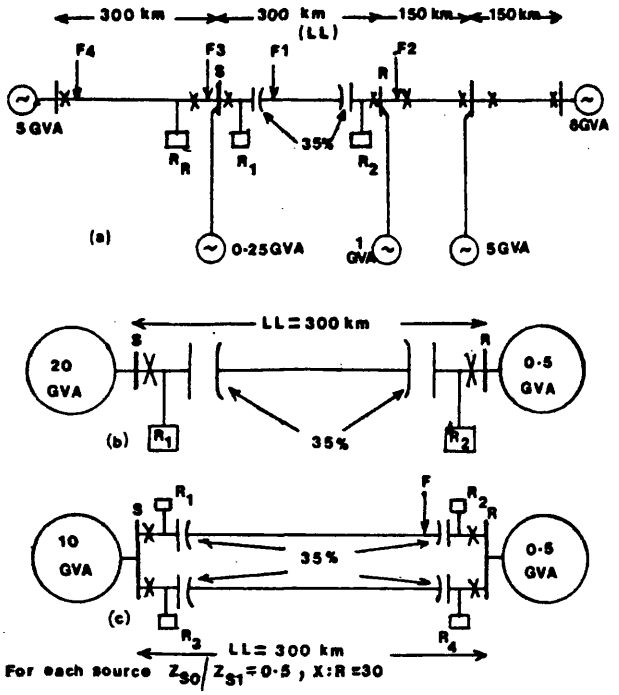


Fig. 3 System configurations studied

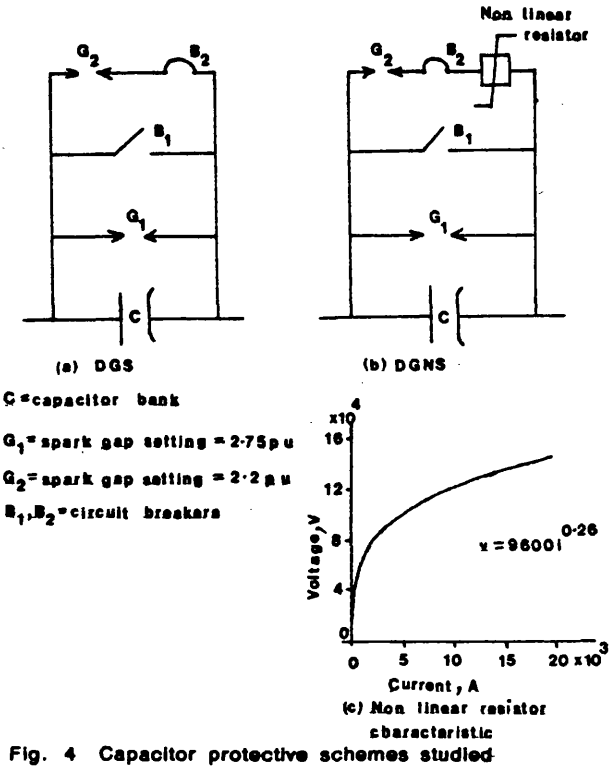


Fig. 4 Capacitor protective schemes studied

arrangement shown in Fig. 3(c).

As regards the capacitor locations, the two most common systems used are: a) a single capacitor bank located at the middle of the line, and b) a capacitor bank located in the vicinity of each line end. Of the two, although the former is economically less viable, however, from a line protection point of view, it is generally more easily protected and does not pose any major problems with modern protection relays. The latter system, however, although economically very attractive, poses some of the most difficult protection problems associated with series compensated systems using present generation relays. The results presented herein are therefore for the system where a capacitor is located near each line end and a typical level of compensation of 70% is used throughout.

In practice, there are a number of capacitor protective schemes in use. In this respect, choice very much depends on the design and operation of a particular power network as well as the usual cost considerations. The two most widely used schemes are the single-gap scheme and the dual-gap scheme (DGS). Of the two, the latter, particularly the one employing a non-linear resistor (DGNS), is finding more widespread use because of its number of distinct advantages over the former [8]. The results presented are for a system employing a DGNS and in order to ascertain the differences in relay performance between DGNS and DGS, a result is also presented for the latter. The two capacitor protective arrangements are as shown in Fig. 4. A typical gap setting of 2·2 p.u. is used throughout.

The relay setting procedures are essentially the same as those outlined in reference [7]. Nominal CT and VT ratios of 1200/1 and $500.10^3/110$ respectively are used throughout and in the case of the VT, a conventional CVT model is used.

RELAY RESPONSE EVALUATION

The modelling techniques used here for obtaining the primary system fault transient waveforms are essentially the same as those outlined in reference [3].

The following apply to all the fault studies illustrated:

(i) v_{ao^o} = negative to positive zero-crossing point of a-phase voltage.

(ii) v_{ao^o} = 30° after the negative to positive zero crossing of a-phase voltage.

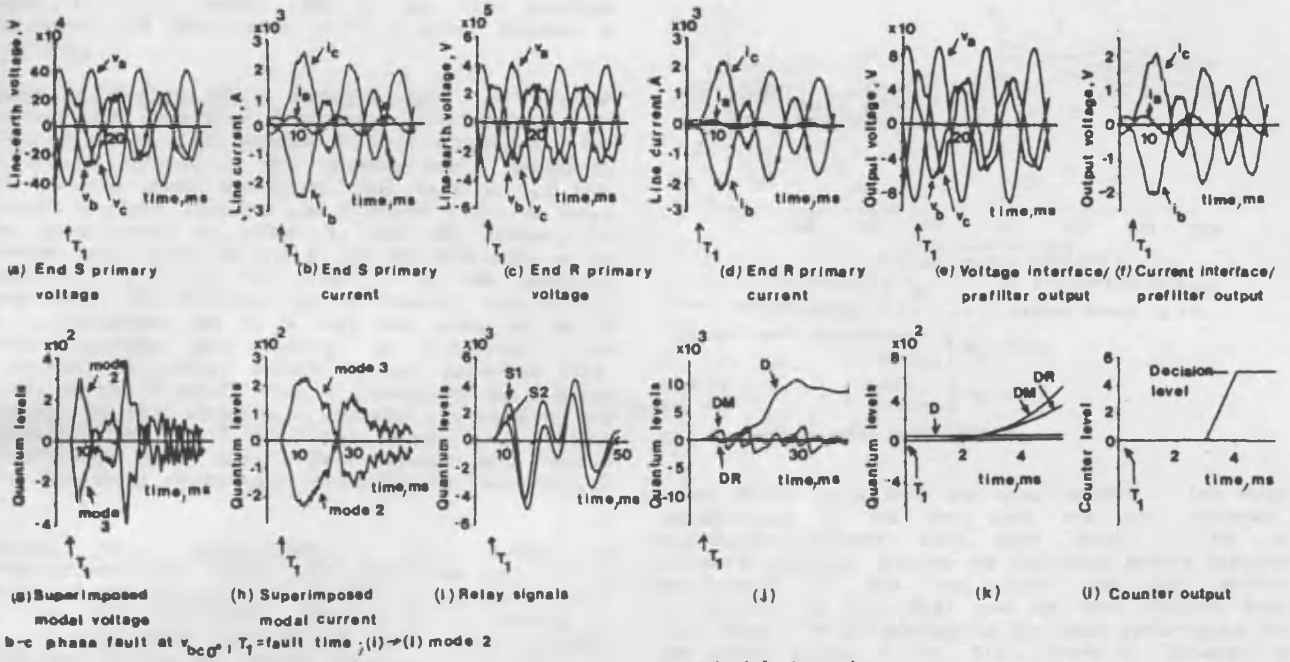
(iii) v_{ao^o} = 90° after the negative to positive zero crossing of a-phase voltage.

(iv) v_{bc^o} = negative to positive zero-crossing point of voltage between b and c phases.

Relay Performance For Internal Faults

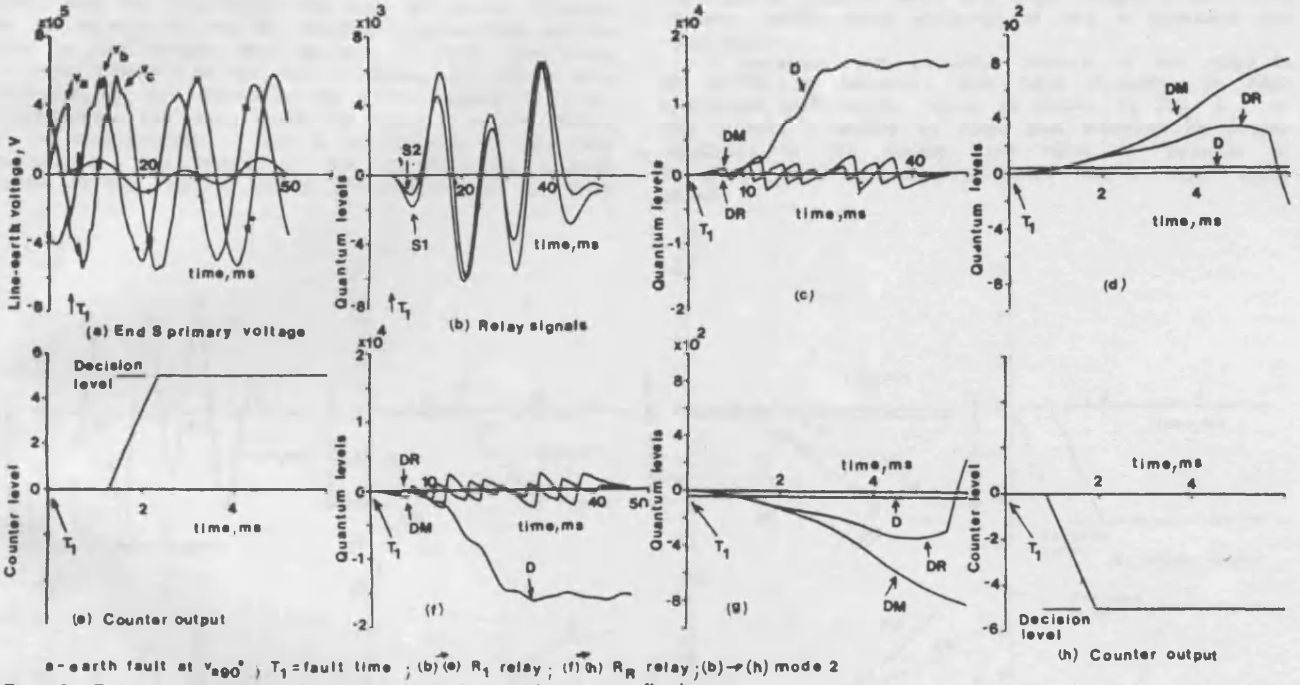
An extensive series of studies of the arrangements of Figs. 3(a) and 3(b) have shown that the relays at both ends S and R give correct HS responses for all types of practically encountered faults on the feeder LL. This is so, irrespective of the precise time(s) after fault at which capacitor gap(s) flashover and also the exact number of flashovers.

A typical fault study: Fig. 5 typifies the waveforms observed at the output of the different processes of the protection scheme, following a b-c phase fault at the mid-point of the line LL for the arrangement shown in Fig. 3(a). This fault condition results in phases b and c capacitor gap flashovers, at both ends S and R, in approximately 6ms and 6.5ms after fault, respectively. Figs. 5(a) - (d) show the primary system waveforms at the two ends. The outputs of the voltage and current interface/prefilter modules at end S, for example, are little different from the primary system waveforms, as shown by Figs. 5(e) - (f). This is somewhat expected because for the fault condition considered, the primary system waveforms are relatively smooth with little high frequency (hf) components. Figs. 5(g) - (h) show the outputs (at point X in Fig. 2) of the complete digital filter arrangement for the R_1 relay. The absence of the prefault steady-state components due to the rejection property of the superimposed extraction filters is clearly evident. Also evident is the fact that for the



b-c phase fault at v_{bc0° ; T_1 = fault time ; (i)→(l) mode 2

Fig. 5 Waveforms at different points in the relay scheme for a typical fault study



a-earth fault at v_{a90° ; T_1 = fault time ; (b)(e) R_1 relay ; (f)(h) R_R relay ; (b)→(h) mode 2

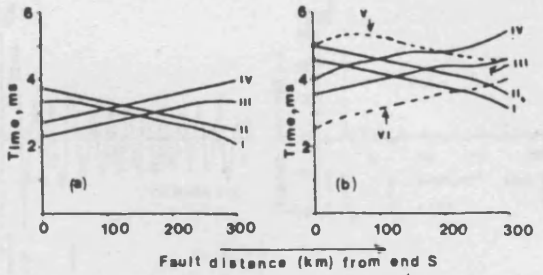
Fig. 6 Relay performance for a close-up fault with no gap flashover

particular type of fault considered. the two modal signals (modes 2 and 3) are almost equal and opposite. This is again as expected. When considering the relay measurands. Fig. 5(i) clearly shows that for this internal fault. the magnitude of signal S1 is greater than that of signal S2. in the initial measuring period. This results in both the magnitude and rate differences (DM and DR respectively) of the two measurands to lie well above the dynamic threshold level D during the measuring period. as evident firstly from Fig. 5(j) and then more clearly from the detailed waveforms of Fig. 5(k). The decision counter quickly attains the required positive level for a forward fault indication. as shown by Fig. 5(l). Also noticeable from Fig. 5(j) is the sharp rise in the dynamic threshold level once the relay has made the initial decision. This is in accordance with the nature of the dynamic function as described in eqn. (10). It should be noted that in this particular study. the outputs of the different processes are illustrated for relay R_1 only. for reasons of brevity. Those for relay R_2

follow a similar pattern and for the fault condition considered, the performance of R_2 is almost identical to that of R_1.

Relay performance for a close-up fault: A potential problem with Directional Comparison schemes based on Distance relays is a possible loss of directionality due to voltage reversal at the relaying point, particularly for close-up faults where the fault level is not high enough to cause capacitor gap flashover. Fig. 6 shows the performances of relays R_1 and R_R following an a-earth fault, close to end S, on the line side of the capacitor (at F1 in Fig. 3(a)). In this particular fault study, the equivalent source capacity level at end S is deliberately set to a very low value so as to inhibit capacitor gap flashover at that end. As expected, the primary system voltage waveforms (Fig. 6(a)) at end S clearly show a reversal of the a-phase voltage, on fault inception. However, in spite of this reversal, both R_1 and R_R relays retain their directionality, i.e. give correct forward and reverse fault indications respectively, as shown by Figs. 6(b) - (h).

Overall relay performance: A series of single-phase-earth faults were simulated at various points on the protected line for the arrangements shown in Figs. 3(a) and 3(b). First of all considering the system configuration shown in Fig. 3(a), it can be seen from Fig. 7 that the overall relay operating times are dependent on the fault inception angle, those for faults near voltage zero being significantly longer than those for voltage maximum faults. This is so because in this relay, both the magnitude and rate differences between the two signals S1 and S2 become progressively smaller (due to the voltage step change on fault occurrence becoming smaller) as the fault inception approaches zero and this in turn prolongs the relay operating time. Furthermore, the relay operating time is also affected by the fault location. This is so because in long line applications, the levels of the voltage and current signals at the relaying points are reduced as the fault



(a) a-earth fault at $V_{a0°}$ (b) a-earth fault at $V_{a90°}$

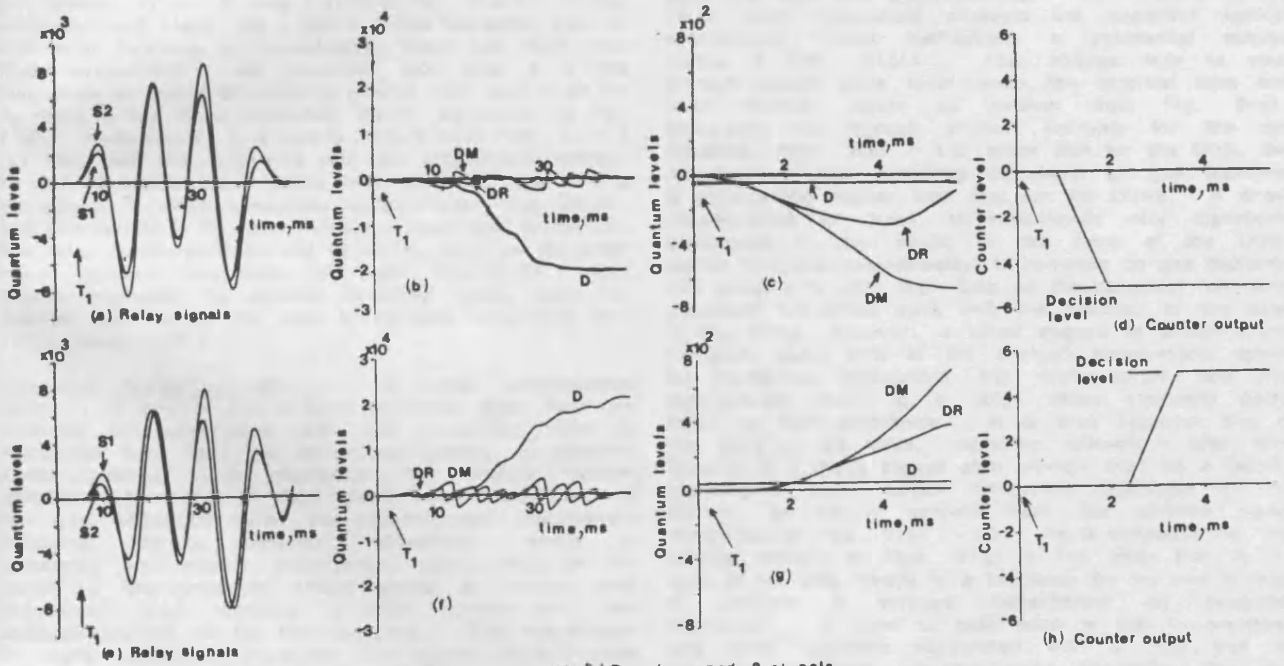
——— system config fig 3 a - - - - system config fig 3 b

(i),(v) fault resistance = 0 ohm
(ii) // // = 100 ohms } R_2 relay
(iii),(vi) // // = 0 ohm
(iv) // // = 100 ohms } R_1 relay

Fig. 7 Overall relay performance

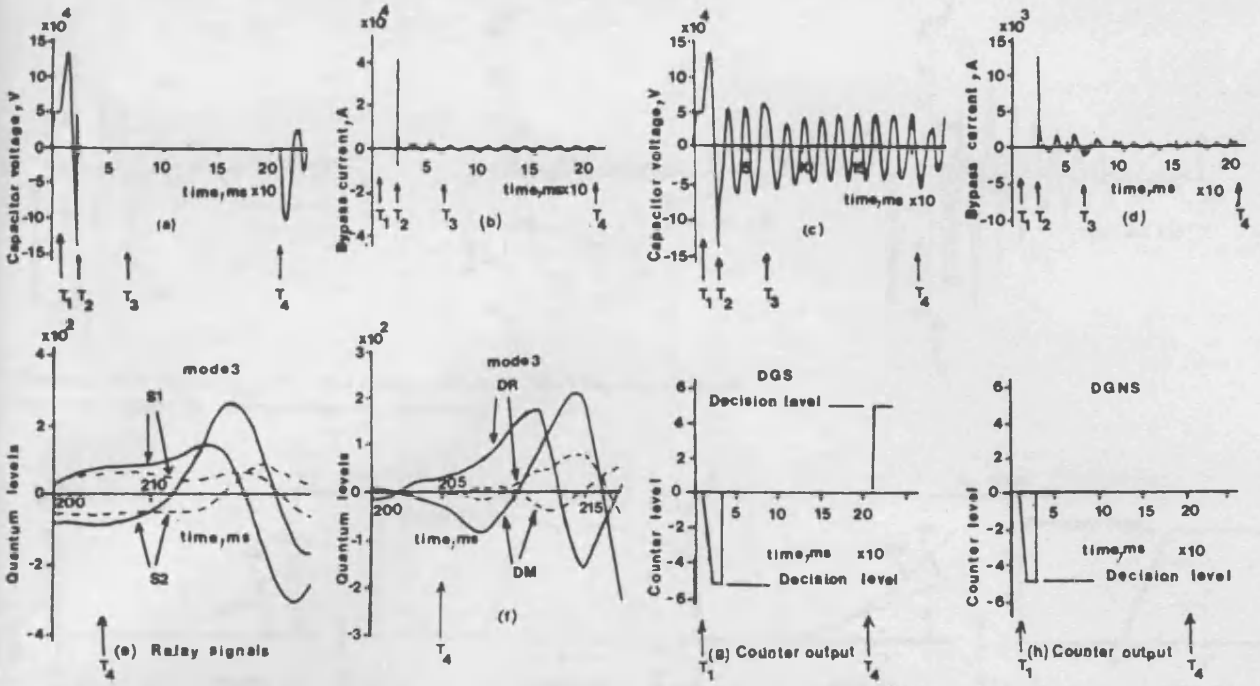
moves further away from the relay location. The relay performances at the two ends are not, however, significantly different from each other. This is somewhat expected because the equivalent source capacity terminations at the two ends for the system configuration of Fig. 3(a) are not very different from each other. When considering the relay performance for the system shown in Fig. 3(b), there is, however, a significant difference in the operating times between the two relays R_1 and R_2, as shown in Fig. 7(b). This is largely because the signals observed at end S, the high source capacity end, are large compared with relay settings, whilst those observed at end R approach the relay setting.

A desirable and attractive feature of the relay is its ability to respond, with high speeds, to high resistance earth faults, again as shown by Fig. 7. In this respect it should be noted that although no longer displaying a HS quality, the relay is capable of detecting much higher resistance faults than those shown.



b-c-earth fault at $V_{a30°}$, T_1 = fault time, (a)→(d) R_2 relay, (e)→(h) R_1 relay; mode 3 signals

Fig. 8 Relay signals for an external fault



a-earth fault at $x_{a90°}$; (a)→(b) and Scapacitor with DGS; (c)→(d) end S capacitor with DGNS; (e)→(h) R_1 relay in (e) & (f) —— = DGS, - - - - = DGNS ; T_1 = fault inception, T_2 = capacitor gap flashover, T_3 = fault clearance, T_4 = capacitor reinsertion

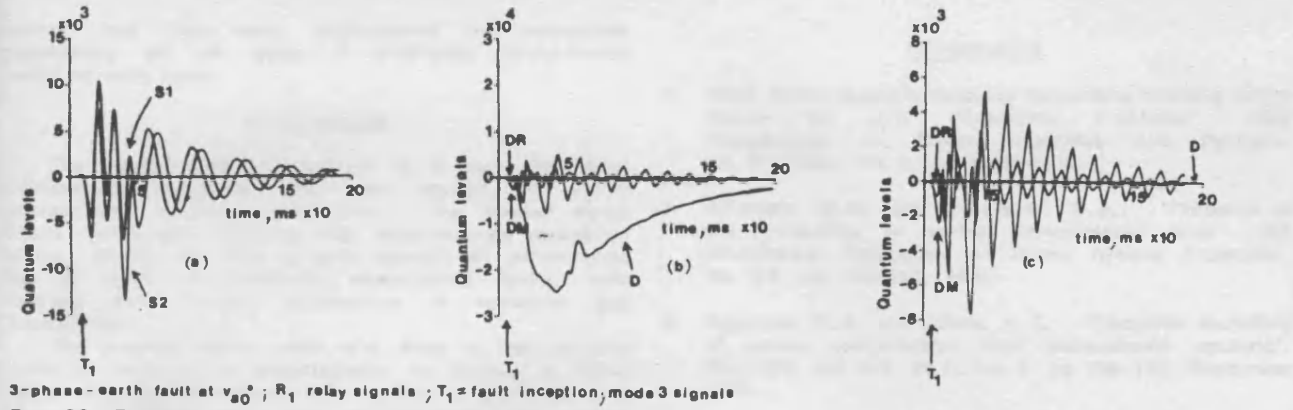
Fig. 9 Effect of capacitor reinsertion

Relay Performance for External Faults

Like the case for internal faults, a series of fault studies using the systems shown in Figs 3(a) and 3(b) have shown that both the relays R_1 and R_2 retain their correct directionality for all types of external faults, again irrespective of capacitor gap flashovers. Fig. 8 shows the relay performance for a double-phase-earth fault just behind the end R relay (at F2 in Fig. 3(a)). In this particular fault study, the c and b phase capacitor gaps at both ends flashover in approximately 15ms and 18ms after fault respectively. As expected, this time it is the magnitude of signal S2 which is greater than that of S1 for R_2 relay in the initial measuring period, as shown by Fig. 8(a). Furthermore, it is clearly evident from Figs. 8(b) - (c) that both the magnitude and rate differences between S1 and S2 exceed the negative threshold level, thus forcing the counter to attain a negative decision level (Fig. 8(d)), and this results in R_2 relay giving a reverse fault indication. The relay measurands S1 and S2 for R_1 relay on the other hand, produce magnitude and rate differences, which having exceeded the positive threshold level, force the counter and hence the relay to indicate a forward fault (Figs. 8(e) - (h)).

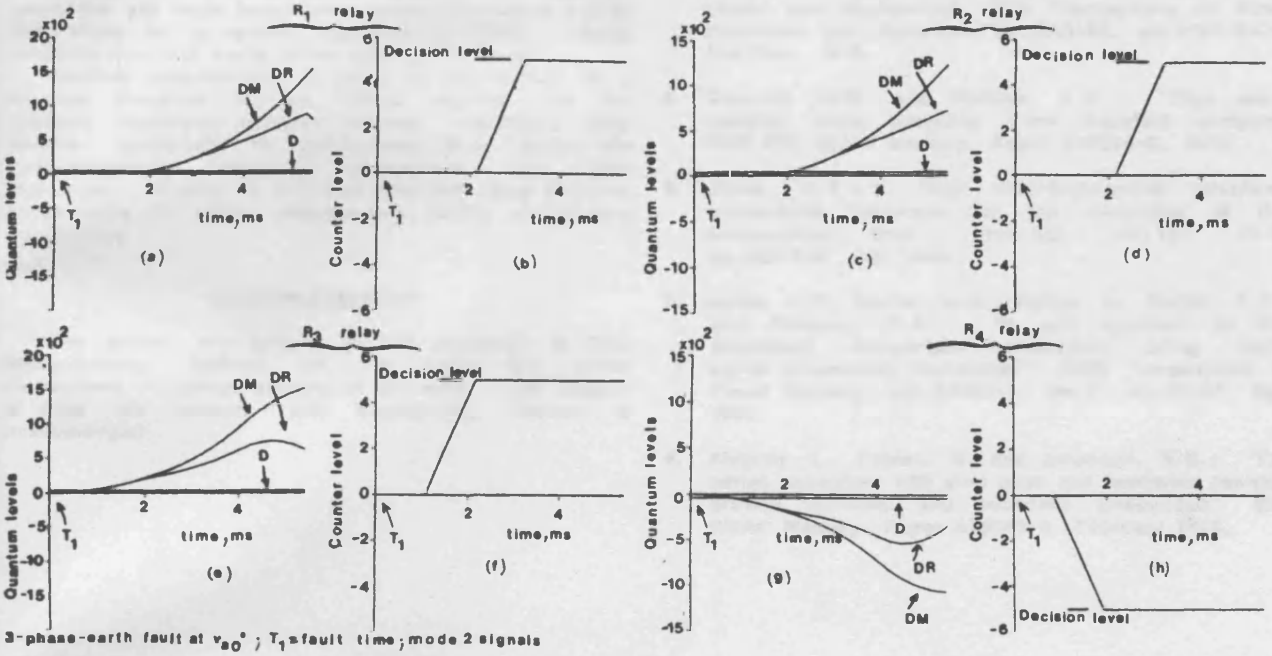
Capacitor reinsertion effects: In series compensated systems, if any of the in-zone capacitor gaps flashover following an out-of-zone fault, the capacitors must be reinserted back into the system as quickly as possible (after external fault clearance) to maintain system stability. However, in high speed relay applications of the type described here, the superimposed components produced during capacitor reinsertion, which is effectively an internal disturbance, can result in the relay on the unfaulted circuit giving a forward fault indication, thus causing a very undesirable and unnecessary trip of the unfaulted line. The magnitudes of these reinsertion transients very much depend upon the type of capacitor protective scheme employed. A better understanding of this transient phenomenon can be achieved by comparing the capacitor voltage and capacitor bypass current waveforms between a system employing a DGS and DGNS.

Figs. 9(a) - (d) show such waveforms for the end S capacitor for an a-earth external fault just behind the end S relay (at F3 in Fig. 3(a)). Comparing the capacitor voltage waveforms first, Fig. 9(a) shows that the DGS causes the capacitor voltage to be clamped down to almost zero after gap flashover and remains so even after the fault has been cleared. The DGNS, on the other hand, adequately protects the capacitor against overvoltages, whilst maintaining a substantial voltage across it (Fig. 9(c)). This voltage falls to near prefault steady state level once the external fault has been cleared, again as evident from Fig. 9(c). Comparing the bypass branch currents for the two schemes, Figs. 9(b) - (d) show that for the DGS, the magnitude of the switching transients on gap flashover is considerably higher than that for the DGNS. A direct consequence of these aforementioned very significant differences is that whilst in the case of the DGS, almost complete compensation is removed on gap flashover and remains so until such time as the capacitor has been physically reinserted back into the system, in the case of the DGNS, however, a small degree of compensation (typically about 20% of the prefault steady-state value) is maintained throughout the fault period and this automatically rises to a large value (typically about 80%) on fault clearance. It is thus apparent that in the case of the DGS, capacitor reinsertion after fault breakoff is a much bigger step change than for a DGNS, resulting in much larger reinsertion transients for the former, as clearly evident from the detailed signal waveforms of Figs. 9(e) - (f). As a consequence, the counter outputs of Figs. 9(g) - (h) show that in the case of the DGS, there is a tendency for the end S relay to indicate a forward disturbance on capacitor reinsertion. A point to note here is that in practice, this relay instability associated with a DGS can be avoided by simply lowering relay sensitivity, but this would be achieved at the expense of reducing its limits of applicability.



3-phase-earth fault at $v_{a0}°$; R_1 relay signals ; T_1 = fault inception; mode 3 signals

Fig. 10 Effect of subsynchronous resonance



3-phase-earth fault at $v_{a0}°$; T_1 = fault time; mode 2 signals

Fig. 11 Relay performance for a fault on a double circuit line

Effect of subsynchronous resonance: The presence of subsynchronous resonance components in the relay measurands, particularly if the level of the fault for an external fault is not high enough to cause capacitor gap flashover, can affect its stability and also prolong relay recovery time thus affecting its ability to respond to an internal fault if such a fault closely follows an external fault. As mentioned before, a dynamic threshold function as opposed to a fixed level has been introduced into the relay design in order to maintain relay stability throughout the period that the subsynchronous resonance components persist.

Fig. 10(a) shows the relay measurands S1 and S2 following a remote-end 3-phase-earth fault behind the relay at end S (at F4 in Fig. 3(a)). There is no gap flashover for this fault. Considering Fig. 10(b), it can be clearly seen that after the initial measuring period, the dynamic threshold level rises sharply and stays well above the signals throughout the period that they are finite and then returns to its minimum level. As can also be seen, the relay is ready to detect another fault approximately 200ms after the first fault. It is interesting to note that if a fixed threshold level (i.e. K_o as shown in eqn. 10) is used, then, as shown by Fig. 10(c), the relay measurands stay well above threshold throughout the entire period that the former are finite. It is thus evident from Fig. 10(c) that a fixed threshold level can cause relay instability under certain external fault conditions.

Double Circuit Line Application Study

A major problem of protecting series compensated double circuit lines using conventional Directional Comparison schemes, particularly those based on Distance relays, is caused by the presence of the second circuit which under certain conditions can cause a voltage or current reversal on the faulted circuit, thus initiating a blocking on this circuit. For example, it can be relatively easily shown that for a 3-phase-earth fault at point F on the double circuit arrangement shown in Fig. 3(c), the current fed via the healthy circuit can cause the current at the relaying point R_1 to reverse [2]. However, with regard to the relay described here, Fig. 11 clearly shows that the relay performs satisfactorily for this type of fault and a series of fault studies for the arrangement of Fig. 3(c) have

shown that the relay performance is completely satisfactory for all types of practically encountered faults on such lines.

CONCLUSIONS

The design and performance of a new Directional Comparison protection relay as applied to series compensated systems is described. The special digital filters developed, including the superimposed extraction filters, enable the relay to give correct HS performance for all types of practically encountered faults, both internal and external, irrespective of capacitor gap flashover(s).

The results clearly show that from a line relaying point of view, it is advantageous to employ a DGNS rather than a conventional DGS. This is particularly so because in cases where the external fault level current is large enough to cause capacitor gap flashover on the unfaulted line, the transients caused by capacitor reinsertion are much larger for a system employing a DGS than those for a system employing a DGNS. Relay instability can thus ensue in the case of the former.

Detailed consideration is given to the design of a dynamic threshold function, which together with the specially developed decision process, maximises relay stability, particularly for out-of-zone faults where the subsynchronous resonance components are quite significant. Finally, it is shown that the relay performs satisfactorily in series compensated double circuit line applications.

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